## EXAMINATION NO. 3

NAME SCORE /75

INSTRUCTIONS: This exam is closed book with one sheet of notes permitted. The exam consists of 3 questions for a total of 75 points. Please show your work leading to your answers so that maximum partial credit may be given where appropriate. Be sure to turn in your exam with the problems in numerical order, firmly attached together.

## Problem 1-( 25 points)

The simplified schematic of a feedback amplifier is shown. Use the method of feedback analysis to find $V_{2} / V_{1}, R_{\text {in }}=V_{1} / I_{1}$, and $R_{\text {out }}=V_{2} / I_{2}$. Assume that all transistors are matched and that $g_{m}=1 \mathrm{~mA} / \mathrm{V}$ and $r_{d s}=\infty$.


## Problem 2-( 25 points)

Use the Blackman's formula (see below) to calculate the smallsignal output resistance of the stacked MOSFET configuration having identical drain-source drops for both transistors. Express your answer in terms of all the pertinent small-signal parameters and then simplify your answer if $g_{m}>g_{d s}>(1 / R)$. Assume the MOSFETs are identical.

$$
R_{\text {out }}=R_{\text {out }}\left(g_{m}=0\right)\left[\frac{1+R R(\text { output port shorted })}{1+R R(\text { output port open })}\right]
$$

(You may use small-signal analysis if you wish but this circuit seems to be one of the rare cases where feedback analysis is more efficient.)


## Problem 3-( 25 points)

Calculate the small-signal voltage gain, the $S R\left(C_{L}=1 \mathrm{pF}\right)$, and the $P_{\text {diss }}$ for the op amp shown where $I_{5}=100 \mathrm{nA}$ and all transistors M1-M11 have a $W / L$ of $10 \mu \mathrm{~m} / 1 \mu \mathrm{~m}$ and $V_{D D}$ $=-V_{S S}=1.5 \mathrm{~V}$. If the minimum voltage across the drain-source of M6 and M7 are to be 0.1 V , design the $W / L$ ratios of $\mathrm{M} 12-\mathrm{M} 15$ that give the maximum plus and minus output voltage swing assuming that transistors M12 and M15 have a current of 50nA. The transistors are working in weak inversion and are modeled by the large signal model of

$$
i_{D}=\frac{W}{L} I_{D O} \exp \left(\frac{v_{G S}}{n V_{t}}\right)
$$

where $I_{D O}=2 \mathrm{nA}$ for PMOS and NMOS and $n_{P}=2.5$ and $n_{N}=1.5$. Assume $V_{t}=26 \mathrm{mV}$ and $\lambda_{N}=0.4 \mathrm{~V}^{-1}$ and $\lambda_{P}=0.5 \mathrm{~V}^{-1}$.


