## Homework Assignment No. 2

Due Wednesday, January 22, 2003 in class
Problem 1-(10 points)
Problem 5.20 of Gray and Meyer. The SPICE parameters to use for this problem are:
.MODEL NPN NPN RB=200 BF=80 IS=1E-18 VAF=130
.MODEL PNP PNP RB=300 BF=20 IS=1E-18 VAF=50
.MODEL PMOS PMOS KP=26U LAMBDA=0.0125 VTO=-0.7 LD=0
Use the following table to summarize your answers for easier grading. (a). Device Currents

|  | Hand Calculations | SPICE Simulations |
| :--- | :--- | :--- |
| $\mathrm{I}_{\mathrm{C} 1}$ |  |  |
| $\mathrm{I}_{\mathrm{C} 2}$ |  |  |
| $\mathrm{I}_{\mathrm{C} 3}$ |  |  |
| $\mathrm{I}_{\mathrm{C} 5}$ |  |  |
| $\mathrm{I}_{\mathrm{C} 6}$ |  |  |
| $\mathrm{I}_{\mathrm{D} 1}$ |  |  |
| $\mathrm{I}_{\mathrm{D} 2}$ |  |  |
| $\mathrm{I}_{\mathrm{D} 3}$ |  |  |

(b). $\mathrm{V}_{\mathrm{o}(\max )}=$ $\qquad$ $\mathrm{V}_{\mathrm{o}(\mathrm{mim})}=$ $\qquad$
$\mathrm{P}_{\text {max }}=$ $\qquad$
(c). SPICE Results

- A plot of the DC transfer characteristic and mark on your results where clipping begins to occur.
- Plots of $\mathrm{i}_{\mathrm{C} 1}, \mathrm{i}_{\mathrm{C} 2}$, and $\mathrm{i}_{\mathrm{D} 2}$ for $\mathrm{v}_{\mathrm{o}}=2 \mathrm{~V}$ peak and $\mathrm{v}_{\mathrm{o}}=4 \mathrm{~V}$ peak. Assume a signal frequency of 10 KHz . (Note: you will have to apply the appropriate dc bias and signal amplitude to achieve the desired output conditions.)
- Also use SPICE to compute the THD of the output voltage for both the 2 V and 4 V conditions.

|  | Hand Calculations | SPICE Simulations |
| :---: | :--- | :--- |
| Clipping |  |  |
| $\max$ |  |  |
| $\min$ |  |  |
| THD of $\mathrm{v}_{\mathrm{o}}$ |  |  |
| 2 V peak | NA |  |
| 4 V peak | NA |  |

## Problem 2-(10 points)

Six versions of a source follower are shown below. Assume that $K_{N}^{\prime}=2 K_{P}^{\prime}, \lambda_{P}=2 \lambda_{N}$, all W/L ratios of all devices are equal, and that all bias currents in each device are equal. Neglect bulk effects in this problem and assume no external load resistor. Identify which circuit or circuits have the following characteristics: (a.) highest small-signal voltage gain, (b.) lowest small-signal voltage gain, (c.) the highest output resistance, (d.) the lowest output resistance, (e.) the highest $v_{\text {out }}(\max )$ and (f.) the lowest $v_{\text {out }}(\max )$.


## Problem 3-(10 points)

A push-pull follower is shown which uses an NPN BJT and a p-channel MOSFET. In this problem, ignore the bulk effect, the channel length modulation, and the Early voltage. The parameters for the NPN BJT are ${ }_{-F}=100, I_{s}=10 \mathrm{fA}$ and $V_{t}=25.9 \mathrm{mV}$. The model parameters for the PMOS are $K_{P}{ }^{\prime}=50 \mu \mathrm{~A} / \mathrm{V}^{2}$ and $V_{T}=-0.7 \mathrm{~V}$. (a.) Find the value of the dc batteries, $V_{1}$ and $V_{2}$, which will cause $100 \mu \mathrm{~A}$ to flow in Q 1 and M 2 when the dc value of $v_{I N}=0 V D C$. (b.) Find the small-signal input resistance, output resistance and voltage gain when the dc value of $v_{I N}=0 \mathrm{VDC}$.


## Problem 4 (40 points) - Design Problem \#1

You are to design a CMOS output amplifier having a single-ended input and singleended output and a voltage gain of +1 . This amplifier is to use $\pm 2 \mathrm{~V}$ power supplies and all W/L values should be between 1 and 100. You may only use MOSFETs or substrate or vertical BJTs (only one type, NPN) in your design with the exception of a load capacitor $\left(C_{L}\right)$ and load resistor $\left(R_{L}\right)$. You should use the following model parameters for SPICE. Use $\beta_{F}=100$ and $I_{s}=10 \mathrm{fA}$ for the BJT.

|  | $K^{\prime}$ <br> $\left(\mu \mathrm{A} / \mathrm{V}^{2}\right)$ | $V_{T}(\mathrm{~V})$ | $\gamma(\sqrt{\mathrm{V}})$ | $2 \phi_{F}(\mathrm{~V})$ | $\lambda\left(\mathrm{V}^{-1}\right)$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NMOS | 110 | 0.7 | 0.4 | 0.7 | $0.04(\mathrm{~L}=1 \mu \mathrm{~m})$ <br> $0.01(\mathrm{~L}=2 \mu \mathrm{~m})$ |
| PMOS | 50 | -0.7 | 0.57 | 0.8 | $0.05(\mathrm{~L}=1 \mu \mathrm{~m})$ <br> $0.01(\mathrm{~L}=2 \mu \mathrm{~m})$ |

The various definitions used in the specifications of this design are:
1.) Slew rate $(S R)$ is the smallest $\pm$ output voltage rate across a 1 nF load capacitance when the output voltage is between $\pm 1 \mathrm{~V}$.
2.) The peak output voltage $\left(V_{P}\right)$ is the minimum $\pm$ deviation from the quiescent output voltage when a sinusoid is applied to the input and a $100 \Omega$ resistor is attached to the ouput.
3.) Efficiency in percent $(\eta)$ is defined as

$$
\eta=\left(\frac{\text { Power to the load resistor of } 100 \Omega}{\text { Power from the supplies }}\right) \times 100
$$

4.) Voltage gain $\left(A_{v}\right)$ is the output voltage (peak-to-peak) over the input voltage (peak-topeak) when the output is loaded with a $100 \Omega$ load resistor.

Your score for this problem will be determined as follows:

$$
\mathrm{SCORE}=1.0 \times 10^{6} \cdot \min [S R, 10 \mathrm{~V} / \mu \mathrm{s}]+10 \cdot \min \left[V_{P}, 1\right]+0.4 \cdot \min [\eta, 25]+\frac{10}{\left|A_{v^{-}}\right| \mid+1}
$$

