## EXAMINATION NO. 2

NAME SCORE /100

INSTRUCTIONS: This exam is closed book with one sheet of notes permitted. The exam consists of 4 questions for a total of 100 points. Please show your work leading to your answers so that maximum partial credit may be given where appropriate. Be sure to turn in your exam with the problems in numerical order, firmly attached together.

## Problem 1-( 25 points)

A self-compensated op amp has three higher order poles grouped closely around $-1 \times 10^{9}$ radians $/ \mathrm{sec}$. What should be the $G B$ of this op amp in Hz to achieve a $60^{\circ}$ phase margin? If the low frequency gain of the op amp is 80 dB , where is the location of the dominant pole, $p_{1}$ ? If the output resistance of this amplifier is $10 \mathrm{M} \Omega$, what is the value of $C_{L}$ that will give this location for $p_{1}$ ? (Ignore any other capacitance at the output for this part of the problem).

## Problem 2-( 25 points)

Design the values of $W$ for each of the transistors of the op amp shown assuming that the channel lengths of all transistors are $1 \mu \mathrm{~m}$. Also design the values of the bias voltages $V_{B N}$ and $V_{B P}$. The transistor model parameters are $K_{N}{ }^{\prime}=300 \mu \mathrm{~A} / \mathrm{V}^{2}, V_{T N}=0.5 \mathrm{~V}$, and $K_{P}{ }^{\prime}=70 \mu \mathrm{~A} / \mathrm{V}^{2}, \quad V_{T P}=$ -0.5 V . Ignore the bulk effects. Use the following constraints among the transistor widths:
$W_{1}=W_{2}, W_{4}=W_{5}, W_{6}=$ $10 W_{4}, W_{7}=10 W_{5}, W_{8}=W_{9}$, and $W_{10}=W_{11}=W_{12}=W_{13}$

Round the values of the transistor
 widths to the nearest integer that meets or exceeds the specifications. Do not use safety factors or worst case in your design. The op amp specifications assuming a load capacitance of 5 pF are:

$$
V_{\text {icm }}{ }^{+}=0.75 \mathrm{~V}, V_{\text {icm }}=-0.25 \mathrm{~V}, G B=200 \mathrm{MHz}, V_{\text {out }}{ }^{+}=0.5 \mathrm{~V}, V_{\text {out }}{ }^{-}=-0.5 \mathrm{~V}, S R=100 \mathrm{~V} / \mu \mathrm{s}
$$

## Problem 3-(25 points)

Assume the following for all transistors: $\mathrm{g}_{\mathrm{m}}=50 \mu \mathrm{~S}, \mathrm{r}_{\mathrm{ds}}=$
$100 \mathrm{~K} \Omega, \mathrm{~V}_{\mathrm{ds} \text { sat }}=300 \mathrm{mV}, \mathrm{V}_{\mathrm{bs}}$ $=0 \mathrm{~V}$, and $\mathrm{C}_{\mathrm{L}}=25 \mathrm{pF}$.
a) Determine the differential small-signal gain at very low frequencies.
b) Determine the Slew-Rate performance.
c) Determine the dominant pole of this circuit.
d) Identify the locations of the non-dominant poles of this circuit (e.g., gate of mnb2b, etc.).


## Problem 4-( 25 points)

a) Identify the node that establishes the dominant pole frequency (e.g., base of Q24, etc.).
b) Identify all the nodes that introduce non-dominant poles in the circuit.
c) What is the purpose of Q15?
d) What is the purpose of Q16?
e) What is the purpose of Q17?
f) What is the purpose of Q7?

g) Is the gain from the base of Q17 to the emitter of Q23A high or low?

Extra Sheet

