EXAMINATION NO. 3
(Average score $=74 / 100$ )

## Problem 1-( 25 points)

Referring to the feedback circuit shown on the right, answer and/or fill in the blanks of the following questions:
a. What kind of mixing is being employed?

Series $\rightarrow\left(V_{i \underline{i n}}-V_{o u t}\right)$
b. What kind of sampling is being employed?

Shunt $\rightarrow$ ( $V_{\text {out }}$ via mn1's CG gain stage))
c. What type of amplifier is the feedback circuit?
$\underline{V}_{\text {out }} / V_{\text {in }} \rightarrow$ Voltage Amplifier
d. $\mathrm{R}_{\text {in }}=\mathrm{R}_{\text {in_open_lopp }} * \quad(\boldsymbol{1}+\boldsymbol{L o o p} \boldsymbol{G a i n})$
e. $\mathrm{R}_{\text {out }}=\mathrm{R}_{\text {out_open_loop }} * \quad 1 \div(1+$ LoopGain $)$
f. Calculate the loop gain of this circuit (assume $\mathrm{r}_{\mathrm{ds}} \rightarrow \infty$ and derive the relationship as a function of small-signal parameters, R , and $\mathrm{A}_{\mathrm{v}}$ ) -hint: break the loop somewhere and compute the transfer function-.

## Opening the loop at the gate of mn2:

LG $=\left(\mathrm{v}_{\mathrm{d} 2} / \mathrm{v}_{\mathrm{g} 2}\right)\left(\mathrm{v}_{\mathrm{d} 1} / \mathrm{v}_{\mathrm{s} 1}\right)\left(\mathrm{v}_{\mathrm{g} 2}^{\prime} / \mathrm{v}_{\mathrm{d} 1}\right)=($ CS gain $)($ CG gain $)\left(\mathrm{A}_{\mathrm{v}}\right)$

$$
=\left(-g_{m 2} / g_{m 1}\right)\left(g_{m 1} R\right)\left(A_{v}\right)=-g_{m 2} R A_{v}
$$

## Problem 2-(25 points)

Referring to the circuit shown, determine the closed-loop output resistance $R_{\text {out }}$ using Return-Ratio (RR) and Blackman's formula:

$$
\mathrm{R}_{\text {out }}=\underline{R}_{\text {out-(Controlled Source Gain=0) }} \frac{*\left(1+\mathrm{RR}_{\text {output port shorted }}\right)}{\left(1+R \mathrm{R}_{\text {output port open }}\right)} .
$$

(Assume $\mathrm{r}_{\mathrm{ds}} \rightarrow \infty, \mathrm{R}_{\mathrm{i}}, \mathrm{R}_{\mathrm{o}}$, and $\mathrm{A}_{\mathrm{v}}$ are the input resistance, the output resistance, and the gain of the differential amplifier. Derive the relationship as a function of smallsignal parameters, $\mathrm{R}_{1}, \mathrm{R}_{2}$, and $\mathrm{A}_{\mathrm{v}}$.)

## Solution

For RR (Loop Gain), break the loop at the gate of mn1:
$R R_{\text {output port shorted }}=0$ (amplifier $A_{v}$ amplifies a " 0 " signal)

$\mathrm{RR}_{\text {output port open }}=\left(\mathrm{v}_{\mathrm{s} 1} / \mathrm{v}_{\mathrm{g} 1}\right)\left(\mathrm{v}_{-} / \mathrm{v}_{\mathrm{s} 1}\right)\left(\mathrm{v}_{\mathrm{g} 1} / \mathrm{v}_{-}\right)=(\mathrm{CD}$ gain $)($ Voltage divider $)\left(\mathrm{A}_{\mathrm{v}}\right)$

$$
=\frac{g_{m 1}\left(R_{1} \|\left[R_{i}+R_{2}\right]\right)}{1+g_{m 1}\left(R_{1} \|\left[R_{i}+R_{2}\right]\right)} \cdot \frac{R_{i}}{R_{i}+R_{2}} \cdot A_{v}
$$

$\mathrm{R}_{\text {out-(Controlled Source Gain=0) }}=\left(1 / \mathrm{g}_{\mathrm{m} 1}\right)\left\|\mathrm{R}_{1}\right\|\left(\mathrm{R}_{2}+\mathrm{R}_{\mathrm{I}}\right)$

$$
=\mathrm{R}_{\text {out_open_loop }} \text { (open loop at gate of mn1) }
$$

Thus:
$\mathrm{R}_{\text {out }}=\frac{\left(1 / g_{m 1}\right)\left\|R_{1}\right\|\left(R_{i}+R_{2}\right)}{\left[1+\frac{g_{m 1}\left(R_{1} \|\left[R_{i}+R_{2}\right]\right)}{1+g_{m 1}\left(R_{1} \|\left[R_{i}+R_{2}\right]\right)} \cdot \frac{R_{i}}{R_{i}+R_{2}} \cdot A_{v}\right]}$

## Problem 3-( 25 points)

A voltage amplifier using feedback around a current amplifier is shown. In this problem assume all of the NMOS transistors are identical. Assume that $R_{1}$ is greater than the transistor transconductance and find the input resistance, $R_{i n}$, the output resistance, $R_{\text {out }}$, the voltage gain, $v_{\text {out }} / v_{\text {in }}$, and the gainbandwidth $(G B)$ in Hz . Assume that the output resistance connected to this voltage amplifier is large.

## Solution



$$
\begin{aligned}
& R_{\text {in }} \approx R_{1}=\underline{\underline{10 \mathrm{k} \Omega}} \\
& R_{\text {out }}=\frac{v_{t}}{i_{t}}, i_{t}=2 \frac{v_{\text {out }}}{R_{2}}=2 \frac{v_{t}}{R_{2}} \rightarrow R_{\text {out }}=\frac{v_{t}}{i_{t}}=\frac{200 \mathrm{k} \Omega}{2}=\underline{\underline{100 \mathrm{k} \Omega}} \\
& i_{\text {in }} \approx \frac{v_{\text {in }}}{R_{1}}+\frac{v_{\text {out }}}{R_{2}} \text { and } i_{\text {out }} \approx-\frac{v_{\text {out }}}{R_{2}}
\end{aligned}
$$

Since $i_{\text {in }}=i_{\text {out }}$, we get

$$
\frac{v_{\text {in }}}{R_{1}}+\frac{v_{\text {out }}}{R_{2}}=-\frac{v_{\text {out }}}{R_{2}} \quad \rightarrow \quad \frac{v_{\text {in }}}{R_{1}}=-2 \frac{v_{\text {out }}}{R_{2}} \quad \rightarrow \frac{v_{\text {out }}}{v_{\text {in }}}=-\frac{R_{2}}{2 R_{1}}=\underline{\underline{-10 \mathrm{~V} / \mathrm{V}}}
$$

The dominant pole is found as,

$$
\begin{aligned}
& p_{\text {dominant }}=\frac{1}{R_{\text {out }} C_{\text {out }}}=\frac{1}{100 \mathrm{k} \Omega \cdot 0.1 \mathrm{pF}}=100 \times 10^{6} \mathrm{rads} / \mathrm{sec} . \\
\therefore & G B=10 \cdot 100 \times 10^{6} \mathrm{rads} / \mathrm{sec} .=1000 \times 10^{6} \mathrm{rads} / \mathrm{sec} . \rightarrow G B=\underline{\underline{159.15 \mathrm{MHz}}}
\end{aligned}
$$

Note: Many tried to work this problem as a feedback problem (which it is) so the results would be achieved from a shunt-shunt feedback network as follows.

The feedback factor would be $f=-1 / R_{2}$ and the amplifier gain would be

$$
a=\frac{v_{\text {out }}}{i_{\text {in }}}=-R_{2} \quad(\text { loop gain is } 1)
$$

Therefore the closed loop gain would be

$$
\frac{v_{\text {out }}}{i_{\text {in }}}=\frac{a}{1+a f}=\frac{-R_{2}}{2}
$$

The desired voltage gain would be

$$
\frac{v_{\text {out }}}{v_{\text {in }}}=\frac{v_{\text {out }}}{i_{\text {in }}} \frac{1}{R_{\text {in }}}=-\frac{R_{2}}{2 R_{1}}=\underline{\underline{-10 \mathrm{~V} / \mathrm{V}}}
$$

The input resistance of the current amplifier is approximately zero, so feedback would give the correct input and output resistances calculated above.

## Problem 4-(25 points)

A differential CMOS amplifier using depletion mode input devices is shown. Assume that the normal MOSFETs parameters are $K_{N}{ }^{\prime}=110 \mathrm{~V} / \mu \mathrm{A}^{2}, V_{T N}=$ $0.7 \mathrm{~V}, \lambda_{N}=0.04 \mathrm{~V}^{-1}$ and for the PMOS transistors are $K_{P}{ }^{\prime}=110 \mathrm{~V} / \mu \mathrm{A}^{2}, V_{T P}=0.7 \mathrm{~V}, \lambda_{P}=0.04 \mathrm{~V}^{-1}$. For the depletion mode NMOS transistors, the parameters are the same as the normal NMOS except that $V_{T N}=-0.5 \mathrm{~V}$. (a.) What is the maximum input common-mode voltage, $V_{i c m}{ }^{+}(\max )$ ? (b.) What is the minimum input common-mode voltage, $V_{i c m}{ }^{-}(\mathrm{min})$ ? (c.) What value of $V_{D D}$ gives an $I C M R=0.5 V_{D D}$ ?


## Solution

$$
\begin{array}{ll}
\text { (a.) } & V_{i c m}{ }^{+}(\max )=V_{D D}-V_{S D 3}(\mathrm{sat})-V_{D S 1}(\mathrm{sat})+V_{G S 1}(50 \mu \mathrm{~A}) \\
& i_{D}=\frac{\beta}{2}\left(V_{G S 1^{-}} V_{T 1}\right)^{2} \rightarrow \quad V_{G S 1}=\sqrt{\frac{2 i_{D}}{\beta}}+V_{T 1}=V_{D S 1}(\mathrm{sat})+V_{T 1} \\
\therefore & V_{i c m}{ }^{+}(\max )=V_{D D}-V_{S D 3}(\mathrm{sat})+V_{T 1}=V_{D D}-\sqrt{\frac{2 I_{D 3}}{\beta_{3}}}+V_{T 1} \\
& V_{i c m}{ }^{+}(\max )=V_{D D}-0.3015-0.5=\underline{V}_{\underline{D D}} \underline{\underline{-0.8015}} \\
\text { (b.) } \quad & V_{i c m}^{-}(\min )=V_{D S 5}(\mathrm{sat})+V_{G S 1}(50 \mu \mathrm{~A})=V_{D S 5}(\mathrm{sat})+V_{D S 1}(\mathrm{sat})+V_{T 1} \\
& V_{i c m}{ }^{-}(\min )=\sqrt{\frac{2 I_{D 5}}{\beta_{5}}}+\sqrt{\frac{2 I_{D 1}}{\beta_{1}}}+V_{T 1}=0.1348+0.0953-0.5=-\underline{\underline{-0.2698 \mathrm{~V}}} \\
\text { (c.) } & I C M R=V_{i c m}^{+}(\max )-V_{i c m}^{-(\min )}=V_{D D}-0.8015+0.2698=V_{D D}-0.5317 \\
\therefore & V_{D D}-0.5317=0.5 V_{D D} \quad \rightarrow \quad V_{D D}=2(0.5317)=\underline{\underline{1.063 \mathrm{~V}}}
\end{array}
$$

