Homework Assignment No. 2

Due Wednesday, January 21, 2004 in class

Problem 1 - (10 points)

a) For the emitter follower output stage shown below, find the value of R_1 for maximum efficiency and find the value of that efficiency. $V_{CC}=-V_{EE}=2.5$V, $V_{CE}(sat)=0.2$V, $R_L=10$kΩ, $V_{BE}(on)=0.7$V.

b) The load resistance R_L is replaced with a capacitor of 100pF. If the input voltage suddenly drops from 2.5V to -2.5V, explain what happens at the output and accurately sketch the output voltage as a function of time, specifying its initial and final values and time interval.

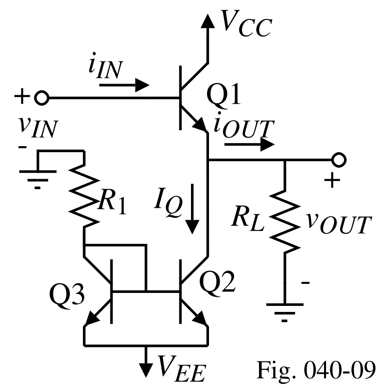
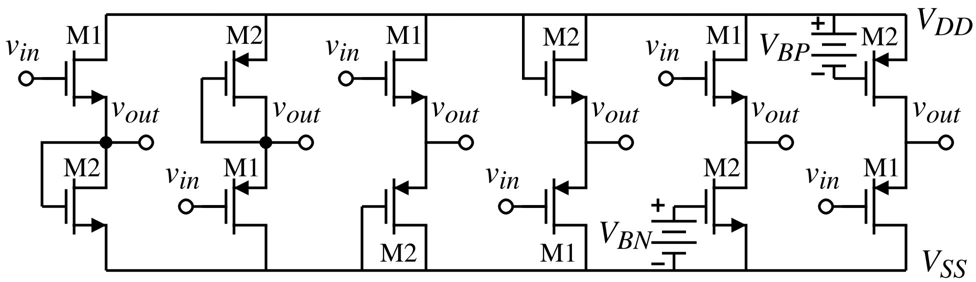


Fig. 040-09

Problem 2 - (10 points)

Six versions of a source follower are shown below. Assume that $K'_N = 2K'_P$, $\lambda_P = 2\lambda_N$, all W/L ratios of all devices are equal, and that all bias currents in each device are equal. Neglect bulk effects in this problem and assume no external load resistor. Identify which circuit or circuits have the following characteristics: (a.) highest small-signal voltage gain, (b.) lowest small-signal voltage gain, (c.) the highest output resistance, (d.) the lowest output resistance, (e.) the highest v_{out}(max) and (f.) the lowest v_{out}(max).



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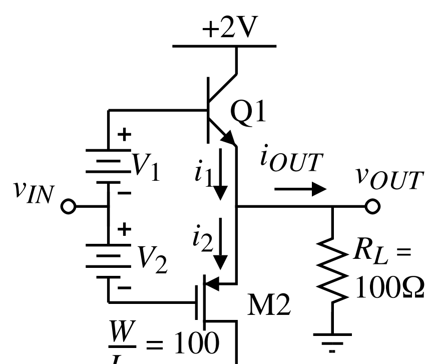
Problem 3 - (10 points)

A push-pull follower is shown which uses an NPN BJT and a p-channel MOSFET. In this problem, ignore the bulk effect, the channel length modulation, and the Early voltage. The parameters for the NPN BJT are β_F = 100, I_s = 10fA and V_t = 25.9mV. The model parameters for the PMOS are K_P' = 50μA/V^2 and V_T = -0.7V. (a.) Find the value of the dc batteries, V_1 and V_2, which will cause 100μA to flow in Q1 and M2 when the dc value of v_{IN} = 0VDC. (b.) Find the small-signal input resistance, output resistance and voltage gain when the dc value of v_{IN} = 0VDC.



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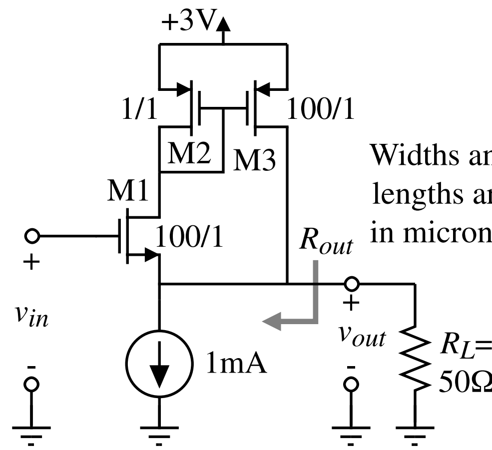
Problem 4 - (10 points)

Find an algebraic expression for the voltage gain, v_{out}/v_{in}, and the output resistance, R_{out}, of the source follower shown in terms of the small-signal model parameters, g_m and R_L (ignore r_{ds}). If the bias current is 1mA find the numerical value of the voltage gain and the output resistance. Assume that K_N' = 110μA/V^2, V_{TN} = 0.7V, and K_P' = 50μA/V^2, V_{TP} = -0.7V.



Widths and lengths are in microns.

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Problem 5 (40 points) - Design Problem #1

You are to design a CMOS output amplifier having a single-ended input and single-ended output and a voltage gain of +1. This amplifier is to use ±2V power supplies and all W/L values should be between 1 and 100. You may only use MOSFETs or substrate or vertical BJTs (only one type, NPN) in your design with the exception of a load capacitor (C_L) and load resistor (R_L). You should use the following model parameters for SPICE. Use β_F = 100 and I_s = 10fA for the BJT.

	K' (μA/V^2)	V_T (V)	$\gamma(\sqrt{V})$	$2\phi_F$(V)	λ (V^{-1})
NMOS	110	0.7	0.4	0.7	0.04(L=1μm) 0.01(L=2μm)
PMOS	50	-0.7	0.57	0.8	0.05(L=1μm) 0.01(L=2μm)

The various definitions used in the specifications of this design are:

1.) Slew rate (SR) is the smallest ±output voltage rate across a 1nF load capacitance when the output voltage is between ±1V.

2.) The peak output voltage (V_P) is the maximum ±deviation from the quiescent output voltage when a sinusoid is applied to the input and a 100Ω resistor is attached to the output.

3.) Efficiency in percent (η) is defined as

$$\eta = \left(\frac{\text{Power to the load resistor of } 100\Omega}{\text{Power from the supplies}}\right)\text{x}100$$

4.) Voltage gain (A_v) is the output voltage (peak-to-peak) over the input voltage (peak-to-peak) when the output is loaded with a 100Ω load resistor.

Your score for this problem will be determined as follows:

$$\text{SCORE} = 1.0\text{x}10^6\cdot\min[SR, 10\text{V}/\mu\text{s}] + 10\cdot\min[V_P, 1] + 0.4\cdot\min[\eta, 25] + \frac{10}{|A_v - 1| + 1}$$