NAME: _____

GEORGIA INSTITUTE OF TECHNOLOGY
School of Electrical and Computer Engineering

ECE 4430	First Exam	Closed Book and Notes
Fall 2002	September 27, 2002	

General Instructions:

1. Write on one side of the paper. (1 Pt.)

2. Put answers to all questions in the spaces provided on the test. (1 Pt.)

3. Show all work for full credit on questions requiring calculations. No credit will be given for answers alone, without supporting work.

4. Problems and questions are weighted as indicated. The maximum score is 100 points.

5. If you need more paper (provided in class), remove the staple from the exam and, when finished, arrange the test in order. Place the extra pages with supporting work in the test behind the page where the problem appears and indicate accordingly. Staple the entire test together so that there are no loose pages. (1 Pt.)

TEST SCORE: _____ / 100

I certify that I have neither given nor received any assistance while taking this test from anyone.

_____ (Signature) (1 Pt.)

☐ Place a check mark in the box if you observed any suspicious actions while taking this test.

Formula Sheet: Equations/Constants that you may, or may not, need are listed below:

$K' = 50\ \mu A/V^2$ (unless otherwise stated in the problem)
$K_n = K'W/L$
$\lambda = 0.01\ V^{-1}$ (unless otherwise stated in the problem)
$V_{TO} = 0.7$ V (unless otherwise stated in the problem)
$\gamma = 0.5\ V^{1/2}$ (unless otherwise stated in the problem)
$2\varphi_F = 0.6$ V (unless otherwise stated in the problem)
$I_{D\text{-}Triode} = (K_n/2)\ [2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$
$I_{D\text{-}Sat} = (K_n/2)\ (V_{GS} - V_{TN})^2\ (1 + \lambda V_{DS})$
$V_{TN} = V_{TO} + \gamma\ [\text{sqrt}(2\varphi_F - V_{BS}) - \text{sqrt}(2\varphi_F)]$
$r_{o\text{-}MOS} \approx 1 / (\lambda I_{DS})$
$g_{m\text{-}MOS} = \text{sqrt}[2I_{DS}K_n]$
$V_{ds\text{-}sat} = \text{sqrt}(2I_{DS}/K_n)$
$g_{mb\text{-}MOS} = \eta g_{m\text{-}MOS}$
$\eta = \gamma \div 2\ \text{sqrt}(2\varphi_F - V_{BS})$

$V_t = kT/q \approx 26$ mV and $I_S = 1E\text{-}15$ A (unless otherwise stated in the problem)
$I_{Diode} = I_S\ [\exp(V_D/V_t) - 1]$

$$C_j = \frac{C_{j0}}{\left(1 - \frac{v_D}{\psi_o}\right)^m} \qquad \rightarrow 0.33 \le m \le 0.5$$

$V_A = 100$ V (unless otherwise stated in the problem)
$\beta_F = 50$ (unless otherwise stated in the problem)
$I_{CE} = I_S\ [\exp(V_{BE}/V_t) - 1]\ [1 + V_{CE}/V_A]$
$r_{o\text{-}NPN} = V_A / I_{CE}$
$g_{m\text{-}NPN} = I_{CE}/V_t$

Device Physics – Part A (38 Points)

1. In a p+n junction diode, if the reverse-biased voltage decreases, the depletion width ***decreases / increases / remains constant***. (2 pts)

2. In a pn junction diode, a high breakdown voltage is caused by _____. The predominant breakdown mechanism in very highly doped diodes is _____ breakdown. (4 pts)

3. ***True or False***: In a p++n junction diode ($N_A >> N_D$), the depletion capacitance is mostly determined by N_A. (2 pts)

4. As the forward-biased voltage of a p+n junction diode increases, the depletion capacitance ***decreases / increases / remains constant***. (2 pts)

5. What physical phenomenon do Early voltage effects describe (qualitatively, what happens to the device)? (4 pts)

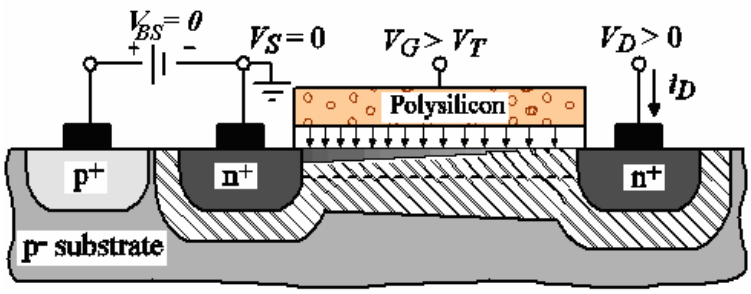
6. The current gain β of an NPN BJT ***decreases / increases / remains constant*** with rising temperatures. (2 pts)

7. ***True or False***: The current gain β of an NPN BJT is dependent on both emitter injection efficiency and base-transport factor. (2 pts)

8. Breakdown voltage BV_{CEO} is ***less than / greater than / equal to*** BV_{CBO}. (2 pts)

9. If a MOS transistor is in the saturation region and its drain current exhibits a linear dependence with respect to gate-source voltage, what physical phenomenon is more than likely occurring?_____. How can a designer ensure a square-law behavior? _____. (6 pts)

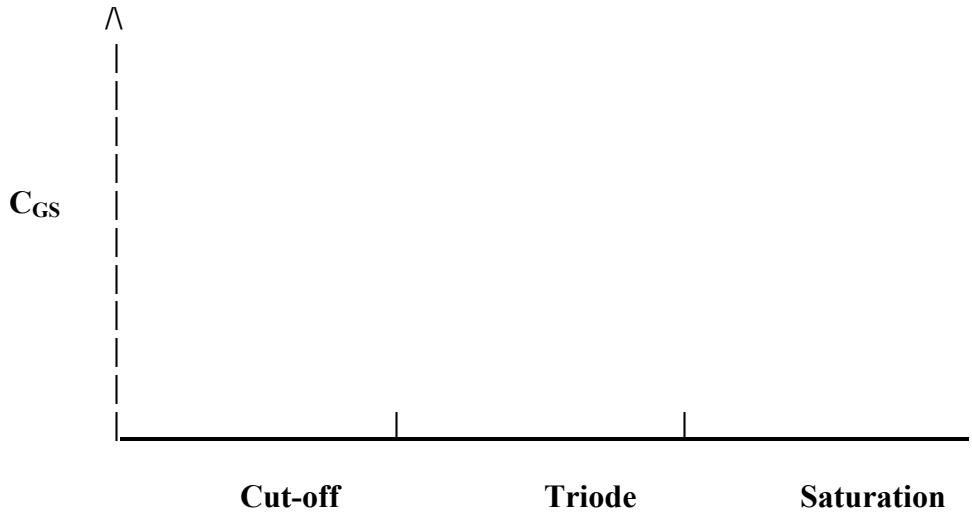
10. In what region of operation is the device shown below operating? _____(2 pts)



11. On the figure above, the effective threshold voltage ***decreases / increases / remains constant*** when the bulk-source voltage V_{BS} is increased from zero to 400 mV. (2 pts)

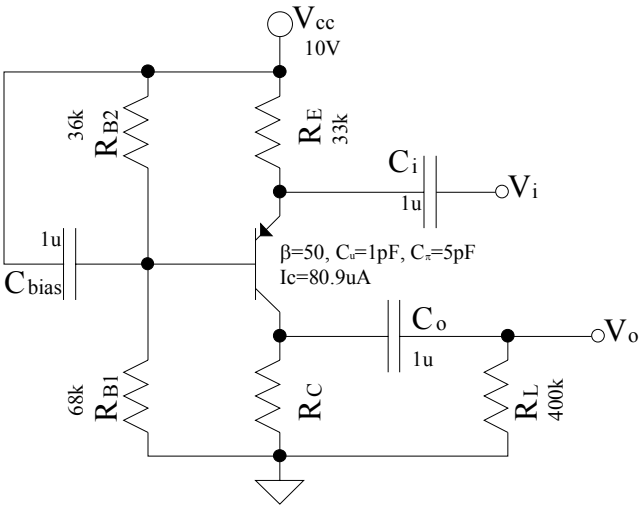
12. If a MOSFET's channel is only weakly inverted, its current is mainly due to ***drift / diffusion / neither***. (2 pts)

13. In the space provided, roughly sketch the value of capacitor c_{gs} as an NMOS device transitions from cut-off, through triode, on to saturation. (6 pts)



Circuits – Part B (42 Points)

1. (a) For the circuit shown below, draw the ac equivalent circuit –do ***NOT*** replace the transistor with its small-signal equivalent model–. (5 pts)

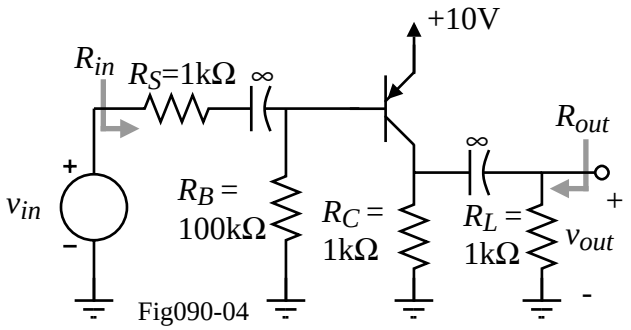


(b) Now replace the PNP with its small-signal model –use only variables, g_m, r_o, r_π, C_μ, C_π, etc., where appropriate and applicable –do ***NOT*** use or calculate their respective absolute values–)–. (5 pts)

2.) As an NPN BJT starts to saturate, capacitor C_μ ***decreases / increases / remains the same***. (2 pts)

3.) ***True or False***: Neglecting high-level injection effects, transition frequency f_t increases with increasing currents for both MOSFETs and BJTs. (2 pts)

4.) (a) Derive the biasing point of the PNP transistor (I_C and V_{CE}) in the figure below if β_F is 75, V_A is 50 V, and the base-emitter voltage is roughly 0.7 V. (8 pts)



(b) Now draw the small-signal equivalent circuit (use variables only, g_m, r_o, r_π, R_S, R_B, R_C, and R_L –do ***NOT*** use or calculate their respective absolute values–). (10 pts)

(c) Now derive the voltage gain from v_{in} to v_{out} ($A \equiv v_{out} / v_{in}$, use variables only, g_m, r_o, r_π, R_S, R_B, R_C, and R_L –do ***NOT*** use or calculate their respective absolute values–). (10 pts)

Device Fabrication – Part C (16 Points)

1.) Given the doping profile shown below, which region(s) has(ve) more than likely been ion implanted? ***1 / 2 / 3 / 4 / 5*** (2 pts)

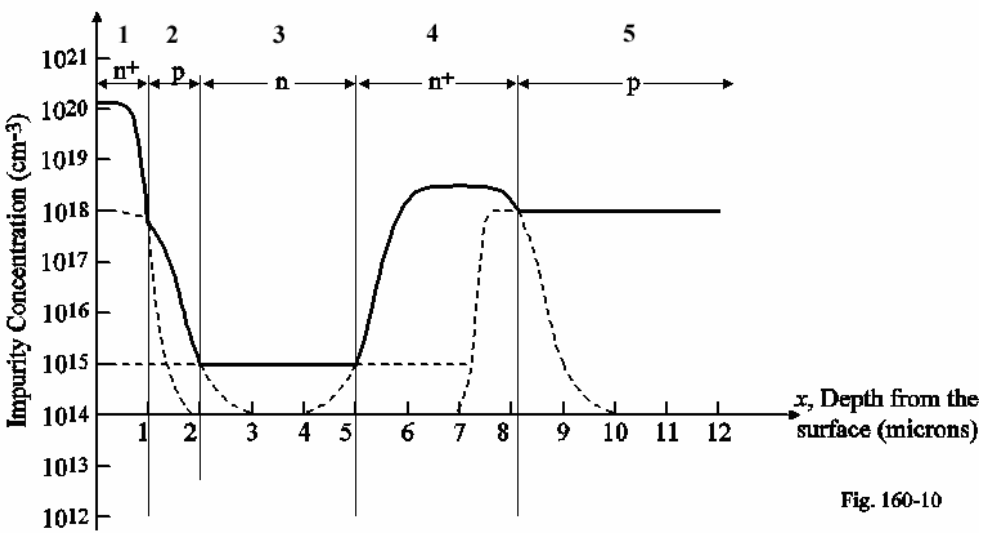


Fig. 160-10

2.) What is the purpose of region 4 –assuming its doping profile was shaped intentionally–? (4 pts)

_____

3.) Given the device below, if the p-base region was used as a large-valued resistor, as shown, where should the collector terminal be connected? ***Positive supply voltage / Negative supply voltage*** (2 pts)

Why? _____

_____ (2 pts)

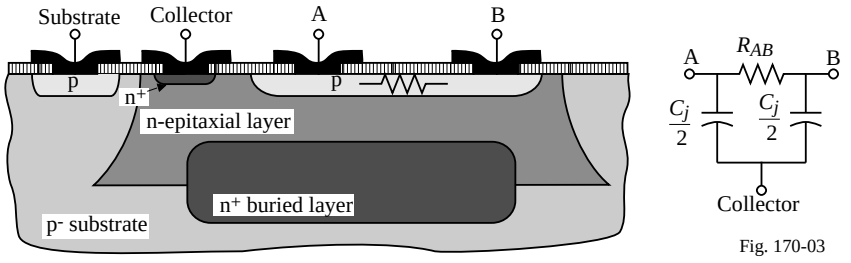


Fig. 170-03

4.) If the collector-base junction was used as a junction capacitor, would adding the n+ buried layer ***increase / decrease / not affect*** its Q performance. (2 pts)

Why? _____(4 pts)

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Part A

① Decreases

② @ Avalanche Multiplication (Impact Ionization)

⑥ Zener

③ False

④ increases

⑤ Effective base-width is modulated, which changes the concentration gradient of minority carriers, which in turn changes the current.

⑥ increases

⑦ True

⑧ Less than

⑨(a) Carrier Velocity Saturation (critical E field has been reached)

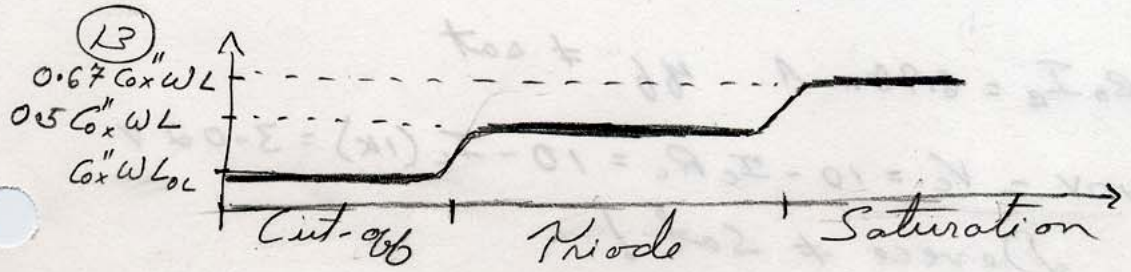
(b) Increase the channel length

⑩ Saturation

⑪ Decreases

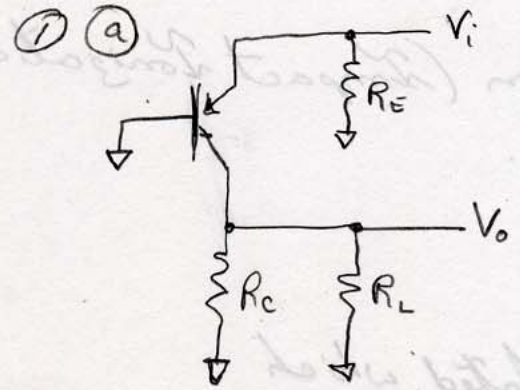
⑫ Diffusion

⑬

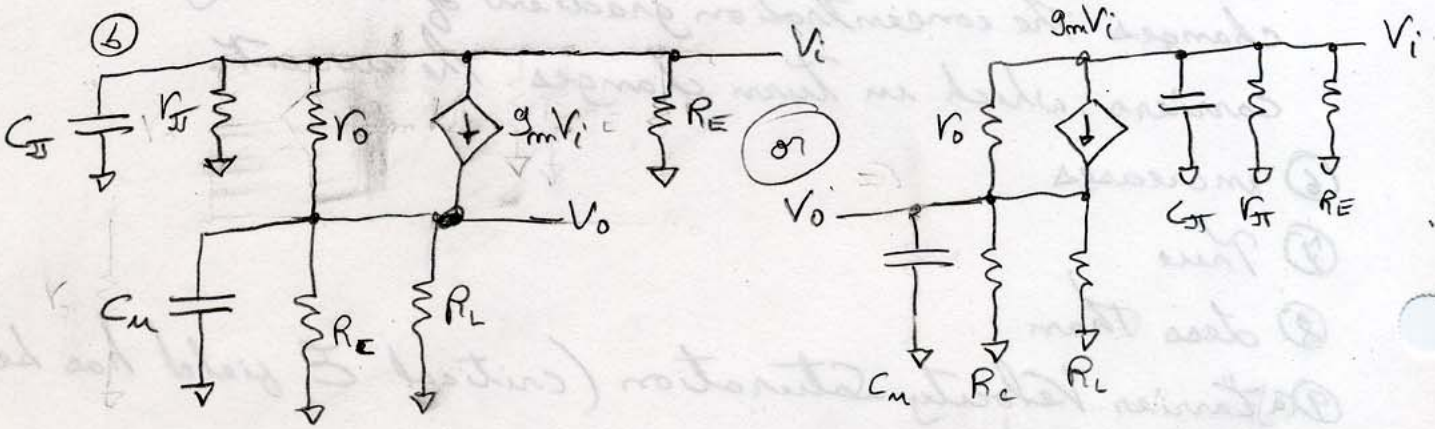


Part B

① (a)



(b)



② Increases (C depletion increases & C diffusion becomes significant → collector-base junction)

③ True ($f_t \propto g_m \propto I_C$ for BJTs $\propto \sqrt{I_D}$ for MOS in sat)

④ (a) $\frac{10V - V_{EB}}{R_B} = I_B = \frac{10 - .7}{100k} = 93\mu A$

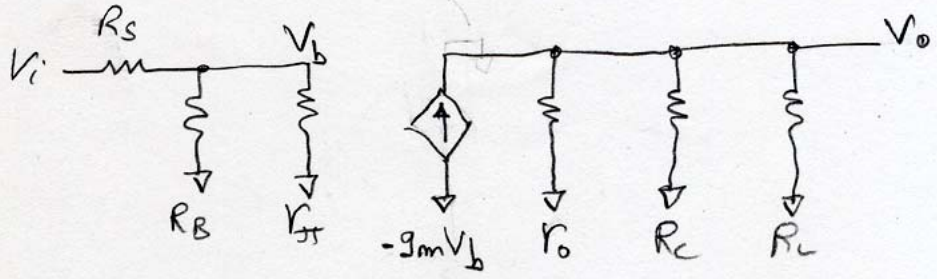
$I_C = \beta_o I_B = 6.98 mA$ ∴ ≠ sat

$V_{CE} = 10V - V_C = 10 - I_C R_C = 10 - I_C(1k) = 3.02 V$

Device ≠ Sat!

Part B

(4) (b)



(c) $$\frac{V_o}{V_i} = \frac{V_o}{V_b}\,\frac{V_b}{V_i} = \left[-g_m\left(r_o \,//\, R_C \,//\, R_L\right)\right]\left[\frac{R_B \,//\, r_\pi}{R_B \,//\, r_\pi + R_S}\right]$$

Part C

(1) 4 for sure and possibly 1

(2) Decrease collector resistance of an NPN.
Degrade forward β of substrate PNP

(3) (a) positive supply
(b) Reverse bias the junction (Isolate device)
Pinch resistance (Increase its value)

(4) (a) Increase (b) (decreases series R - ↓ ESR)