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Cloaking the non-idealities of DC-DC converter stability

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In the world of battery-powered electronics, total chip integration translates to compact, flexible, and low cost solutions, in other words, the ideal products. Power supply circuits, unfortunately, present difficult integration challenges in the form of power density and delivery, which result in the use of large and bulky external power components. What is more, the design values of the power passives and their relevant parasitic components, like equivalent series resistance (ESR) and equivalent series inductance (ESL), vary significantly from one application to the next, on top of their process-, temperature-, frequency-, and drift-over-time dependencies. Ensuring the system is stable over such a wide range of L-C-ESR values is difficult, and in many cases, next to impossible. Switching power supplies are therefore relatively slow and only stable for a narrow band of applications and LC components.

Masking ESR variance

The effect of the output capacitor's ESR on the frequency response of a switching DC-DC converter supply circuit is a left-hand plane (LHP) zero anywhere from moderate to high frequencies, depending on its value, which in turn depends on manufacturer, temperature, and drift performance. Consequently, a designer can neither depend on its existence to maximize phase-margin performance or allow the regulator's bandwidth to reach those frequencies because the zero would otherwise extend the unity-gain frequency (UGF) to regions where parasitic poles exist, compromising the overall stability of the system.

One way to circumvent these ESR design constraints, however, is to mask the zero by bypassing the output capacitor at moderate frequencies with a feed-forward path [1], as illustrated in Fig. 1 [2]. At low frequencies, C_1-R_F bypass filter is high impedance and therefore "transparent," yielding a typical L-C-ESR frequency response. As frequencies increase, however, before the onset of the ESR zero, C1 shorts and feeds more of the ac signal directly to C_F, bypassing output capacitor C and its ESR zero in the process. As a result, the L-C-ESR path is high impedance near the vicinity of the ESR zero, having little to no impact on the overall frequency response of the circuit beyond this point; in other words, the bandwidth and phase-margin response of the system are independent of the ESR zero.

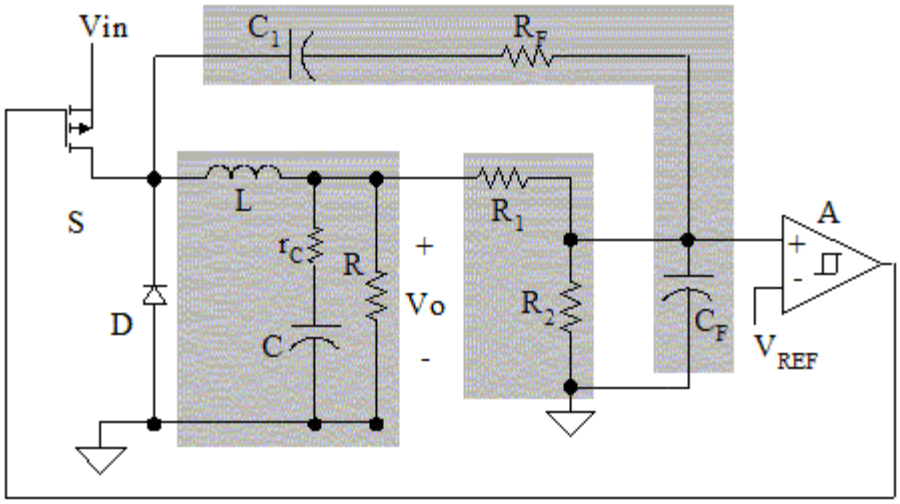

Figure 1. Sample embodiment of a masking feed-forward path (C1-RF)

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The net result of the feed-forward path is the addition of a predictable and relatively low frequency LHP zero. The feed-forward path, in essence, has lower gain than the LC path at lower frequencies and higher gain at higher frequencies, as illustrated by the relative placement of the light solid (main path) and dashed (bypass path) traces of Fig. 2. Since the Y-axis of the Bode plot is in dB, the path with the higher gain determines the combined frequency response of the overall circuit, as shown by the solid dark trace of Fig. 2. At the frequency where the gains of the main and feed-forward paths cross, an ESR-independent LHP zero consequently appears (z_{FF}). The main drawback to this technique is increased output impedance at high frequencies, where the output voltage is masked from the circuit, which translates to slower response times to fast load-dump events.

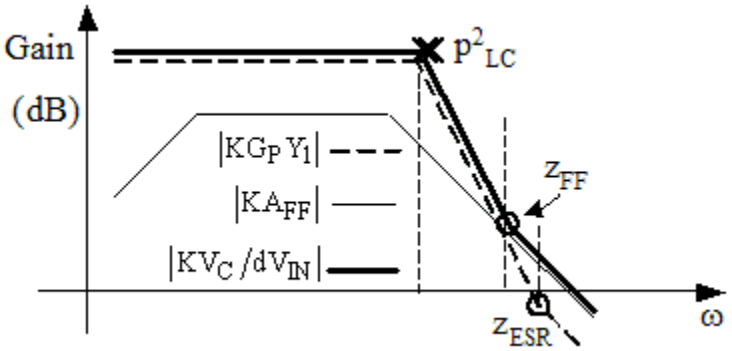

Fig. 2. Bode-plot response of the masking feed-forward path

Eliminating the RHP zero

In boost and buck-boost converter topologies, an oppositely phased feed-forward signal exists, which amounts to a zero but with opposite polarity. The zero appears because the output is temporarily disconnected from the inductor during the energy-storage phase of the converter cycle (e.g., S_M is short- and D_M and S_{AUX} are open-circuited in Fig. 3 -- energy is transferred to the output in a separate phase, when S_M and S_{AUX} are open- and DM is short-circuited). Since a positive load dump (i.e., quick low-to-high level load-current transition) demands more energy, the feedback control loop increases the energy-storage phase, during which time the output is disconnected and discharged by the load. This discharging effect opposes the purpose of increasing energy in the system and therefore amounts to a “parasitic” oppositely phased feed-forward event, otherwise known as a right-hand plane (RHP) zero. The frequency location of this zero depends on inductor L and load resistance R [3].

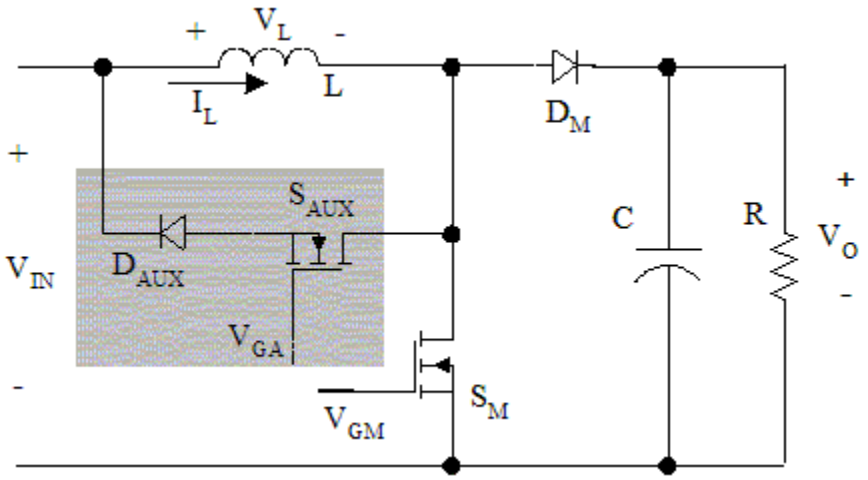

Fig. 3. The use of an auxiliary switch to eliminate the RHP zero in boost converters

The problem is not necessarily that the output is disconnected from the inductor but that the disconnect time is modulated with the feedback control signal; in other words, the disconnect time carries ac information. Consequently, if the disconnect time were to remain constant, the RHP zero path would be eliminated. To do this, a third phase can be introduced to the boost converter cycle whereby the inductor stands-by long enough to ensure the total disconnect time is constant, which is the purpose of S_{AUX} and D_{AUX} in Figure 3. The first and last phases, as before, are the energy-storage and -transfer phases, where S_M and D_M switch and S_{AUX} remains open-circuited. The middle phase occurs when switch S_{AUX} is engaged, short-circuiting the inductor and therefore allowing the inductor current to freewheel, in the meantime letting the load discharge output capacitor C. This additional discharge time is modulated to ensure the total discharge time, which is the sum of S_{AUX}'s and S_M's on-times, is constant, thereby eliminating the RHP zero. The drawbacks to this technique are complexity and, more importantly, increased power losses, since the additional phase increases the average inductor current.

Another means through which the RHP zero can be avoided is by only sensing the output signal when the inductor is connected to the load, masking the oppositely phased ac feed-forward effects seen during the disconnect time. This can be achieved by sensing the peak output voltage of an ESR-dominant capacitor response, as shown in Fig. 4 [4]. Instantaneous positive peak output voltage E increases monotonically with an increase in energy-storage time because the instantaneous current supplied to output capacitor C and its ESR at the onset of the energy-transfer phase is independent of disconnect time. Trough D, on the other hand, which occurs at the end of the disconnect phase, first decreases before increasing, which is a transient embodiment of the oppositely phased feed-forward effect. The drawback to this method is its narrow range of ESR stability.

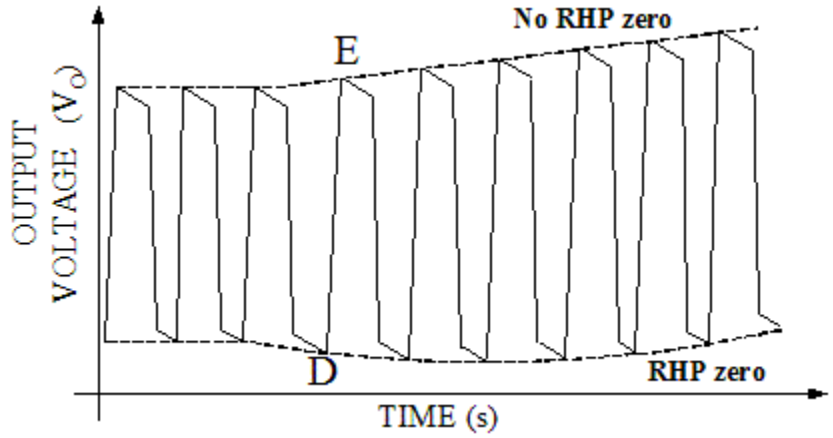

Fig. 4. Asymmetrical peak-trough response of an ESR-dominant boost converter

Increasing LC compliance

LC variations can be accommodated by inserting a servo (feedback) control loop around the filter to ensure and regulate the overall frequency response of the system to a fixed profile. Figure 5 is a block-level illustration of this, whereby the output of forward LC power filter V_{OC} (s) is fed back to a nominal, pre-determined (that is, pre-programmed) inverse LC

response circuit (G_{AUX} (s) = V_{OCNOM}-1(s)) and whose output is ultimately mixed with the error amplifier [5]. The servo loop therefore modulates error signal e(s) to ensure the combined forward frequency response of the LC filter with load resistor R is equal to referenced frequency response V_{OCNOM} (s). The drawback to this fixed LCR response scheme, however, is circuit and frequency compensation complexity, possibly introducing instabilities to boost and buck-boost converters plagued with the RHP zeros and limiting overall bandwidth response.

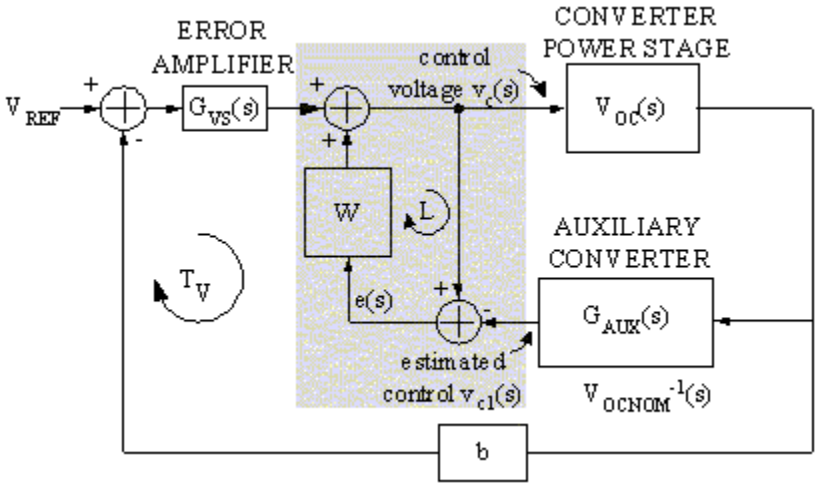

Fig. 5. Regulated (fixed) LCR filter response scheme

Another method of addressing the LC variance of the output filter is by partitioning the LC range into various operating points and designing a programmable compensation circuit tuned to the various LC combinations [6]. Each operating ("grid") point and its respective control equations are designed independently to yield optimum performance. This programmability can be achieved by inserting a digital-signal processor (DSP) in the feedback loop. The two main disadvantages here are guaranteeing stability during all grid-point transitions and limited bandwidth, since numerous clock cycles are required to process any information in the loop and this delay translates to loop-response time [7].

In hindsight

The main challenge in power supply circuits is guaranteeing stability over a wide range of LC and load combinations. The effects of this variance and the non-idealities of the components manifest themselves in the form of variable LC complex-conjugate poles, LHP ESR zeros, and RHP zeros. Masking the ESR zero by adding a bypass feed-forward path is effective, in spite of slightly increasing the output's response time to fast load-dump events. Eliminating the RHP zero by introducing an additional phase in the converter cycle to ensure the discharge time is constant, on the other hand, often increases design complexity and power losses to prohibitive levels. Alternatively, sensing the peak output voltage of ESR-dominant converters to mask the RHP zero effects is less costly but narrow in scope, especially when considering low ESR capacitors are growing in popularity. Finally, increasing LC compliance by inserting an LC-servo loop and/or by adding programmability to the filter circuit is necessarily complex and ultimately slow, and especially risky during operating-point transitions. Masking through feed-forward bypass paths may be the most practical solutions…but that depends on the application.

For additional details, questions, and/or comments on this article, please contact the Georgia Tech Analog and Power IC Design Lab at gtap@ece.gatech.edu. More information about our research can also be found at http://www.rincon-mora.com/research.

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