

GEORGIA INSTITUTE OF TECHNOLOGY
School of Electrical and Computer Engineering

Course ECE 2040

Circuit Analysis

Assigned: February 25, 2000

Due: March 3, 2000

Problem Set #7

Reading: Read the following sections from the class notes:

Chapter 5, Section 5.5.2, 5.5.3

Chapter 6, Sections 6.1

Reading: Read the following sections from Irwin and Wu:

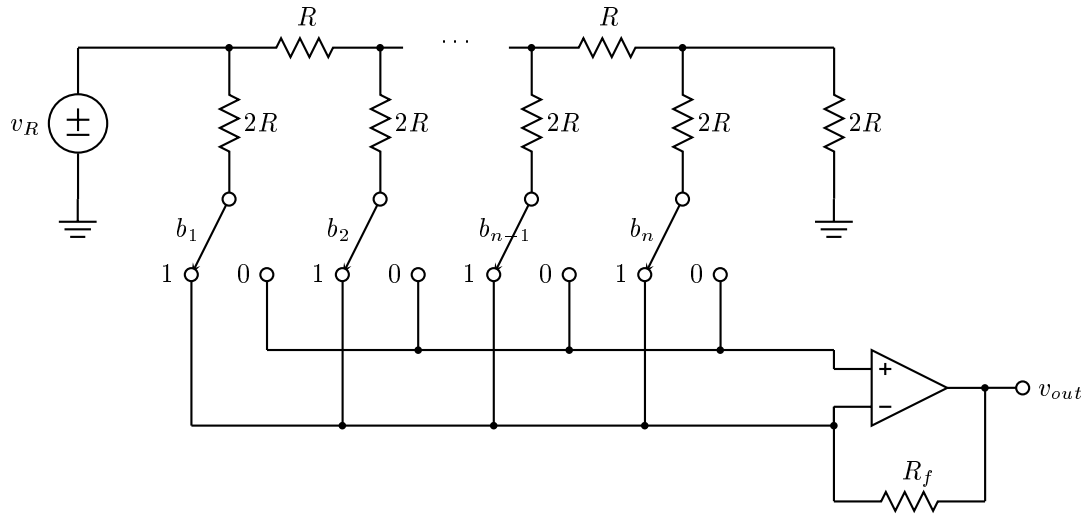
Chapter 13, Sections 13.5 (inverse Laplace transforms)

Chapter 14, Sections 14.1, 14.2, 14.3 (circuits in the Laplace domain)

Problem 7.1: The circuit shown below is called the inverted $R - 2R$ ladder digital-to-analog converter (DAC). The input to this circuit is a binary code represented by b_1, b_2, \dots, b_n , where b_i is either 1 or 0. Each switch shown in the figure is controlled by one of the bits in the binary code. If $b_i = 1$, that switch will be in the '1' position; if $b_i = 0$, that switch will be in the '0' position. Depending on the position of the switch, each current i_k is diverted either to true ground (adding to the + terminal of the opamp) or to the virtual ground (adding to the - terminal.)

- If i is the current flowing out of the voltage source, show that $i = v_R/R$ regardless of the digital input code.
- Show that the output voltage can be expressed as

$$v_{out}(t) = -\frac{R_f}{R}v_R(b_12^{-1} + b_22^{-2} + \dots + b_{n-1}2^{-n+1} + b_n2^{-n})$$



Problem 7.2: Find the inverse Laplace transforms (for $t \geq 0$) for the following functions:

- (a) $X_a(s) = \frac{s^2}{(s+1)^2+1}$
- (b) $X_b(s) = \frac{s+1}{s^2(s+2)}$

Problem 7.3: For the circuit in Figure 1, determine $v_c(t)$ if $i_s(t) = u(t)$. Assume that $v_c(0) = 0$.

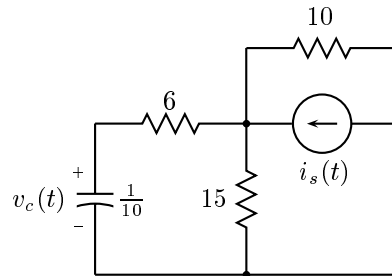


Figure 1: Circuit for Problem 7.3.

Problem 7.4: For the circuit in Figure 2, let $i_s(t) = 1$ for $t > 0$ and assume that at $t = 0$ the current through the inductor is zero and the voltage drop on the capacitor is 1 volt.

- (a) Redraw the circuit in the Laplace domain.
- (b) Determine $V(s)$, the Laplace transform of the resistor voltage.
- (c) Determine $v(t)$ for $t > 0$.

Problem 7.5: The circuit in Figure 3 is at initial rest. This means that at $t = 0$ there is no current flowing through the inductor and no voltage drop across the capacitor. Determine $v(t)$ for all t if $i_s(t) = 2e^{-3t}u(t)$.

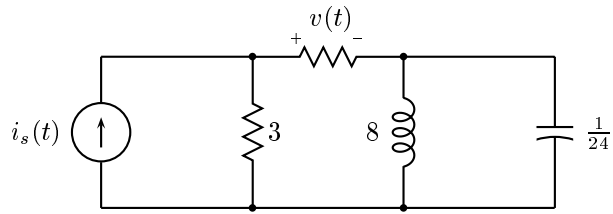


Figure 2: Circuit for Problem 7.4.

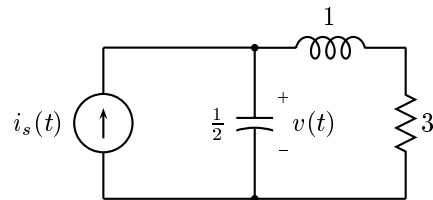


Figure 3: Circuit for Problem 7.5.