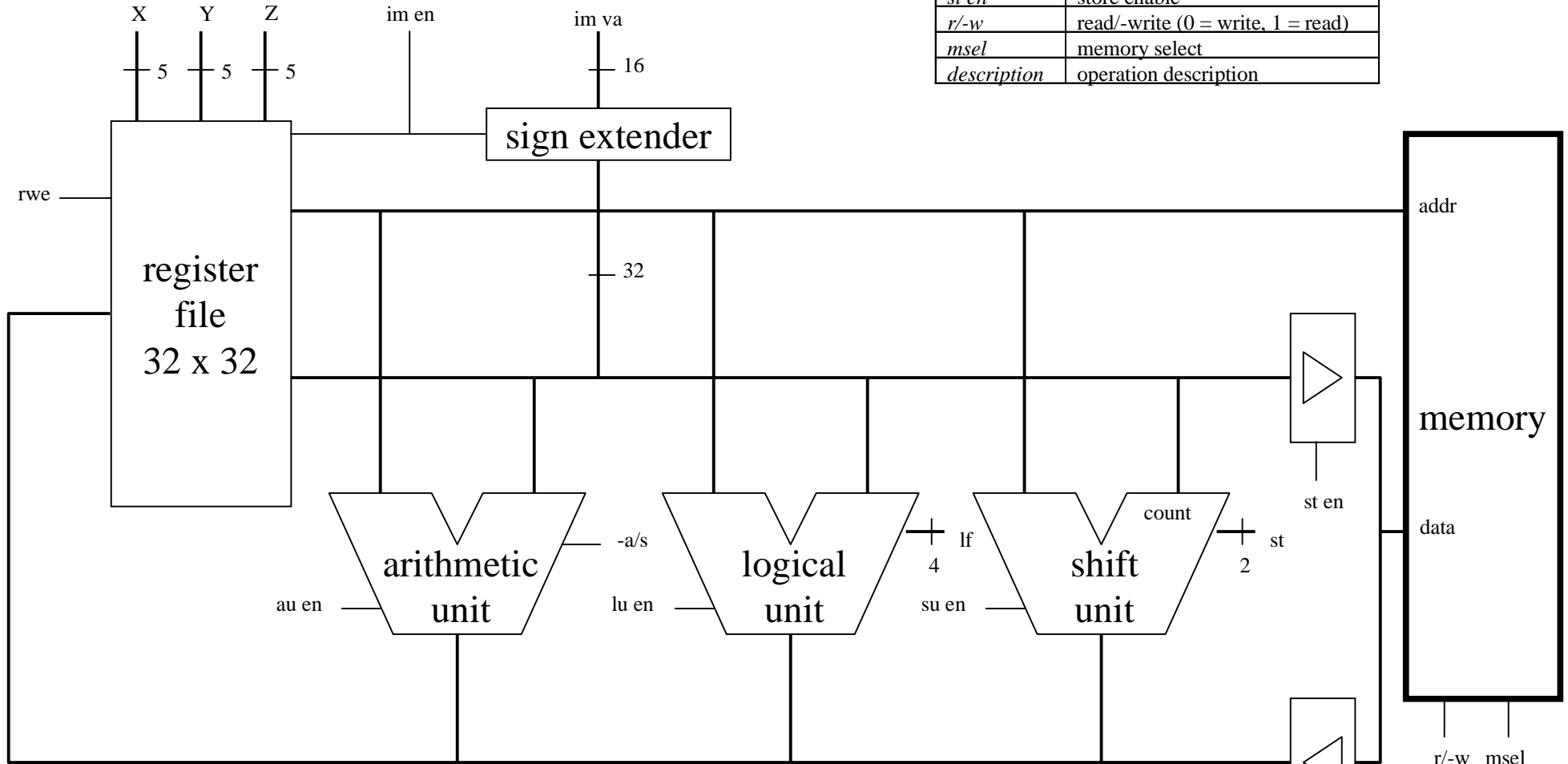


<i>cycle</i>	cycle number
<i>X</i>	register driven onto X bus
<i>Y</i>	register driven onto Y bus
<i>Z</i>	register written from Z bus
<i>rwe</i>	register write enable
<i>im en</i>	immediate enable on Y bus
<i>im va</i>	immediate value

<i>au en</i>	arithmetic unit enable
<i>-a/s</i>	-add / sub (0 = add, 1 = subtract)
<i>lu en</i>	logical unit enable
<i>lf</i>	logical function
<i>su en</i>	shift unit enable
<i>st</i>	shift type
<i>ld en</i>	load enable
<i>st en</i>	store enable
<i>r/-w</i>	read/-write (0 = write, 1 = read)
<i>m sel</i>	memory select
<i>description</i>	operation description



logical functions

X	Y	out
0	0	lf <sub>0</sub>
1	0	lf <sub>1</sub>
0	1	lf <sub>2</sub>
1	1	lf <sub>3</sub>

shift types  
0 = logical  
1 = arithmetic  
2 = rotate  
+ count shifts right  
- count shifts left