

In this exam, you will consider several issues in microprocessor implementation. Here are the "rules" of this exam.

- (1) All work should be your own. Do not discuss the paper, the questions, or your responses with anyone (e.g., classmates, officemates, roommates, soulmates, faculty, mom and dad). I am available for clarification of the questions. However, I will avoid discussions of your responses.
- (2) You should limit your work on this exam to no more than six hours.
- (3) Answer questions using complete sentences. When equations are used, they should be complete with all terms defined.
- (4) Electronic submission: Exams should be written in PDF format and e-mailed as an attached file to scott.wills@ece.gatech.edu. *For this exam only, MS Word 97 format will also be accepted.*
- (5) Page Limit: Limit your responses to FOUR 8.5 x 11 inch pages (excluding a cover page) in a 12 point font with one inch margins. The cover page should follow the following example:

EE 6175 Midterm Exam

George P. Burdell

1	2	3	4	total

- (6) Deadline: Your exam is due Tuesday, 2 February at 5:00pm. Exams will not be accepted after this time. Video students are handled specially.

Have questions? Send me e-mail at scott.wills@ece.gatech.edu.

Good Luck!

QUESTION ONE: (40 points) Consider the following model of superscalar execution (assume a the baseline execution architecture discussed in class).

- (1) The superscalar factor is S .
- (2) The pipeline has five stages: fetch, decode, dispatch, execute, and commit
- (3) The probability that the N th instruction can issue in a given cycle is $(0.7)^N$. This approximates the combined impact of structural and data hazards. This does *not* include the impact of in-order issue (i.e., if instruction I_n does not issue, the probability of I_n issuing is zero.
- (4) 20% of instructions are conditional branches.
- (5) The branch prediction accuracy is 93%.
- (6) Assume no stalls (beyond the issue probability in (3)) from structural or data hazards.
- (7) Branch predicates are computed in a one cycle execution.
- (8) Instructions caused by mispredicted branches are canceled and the correct fetch target is passed to the fetch unit on the cycle following the branch predicate computation.

Part 1.A: Ignoring mispredicted branches, plot instruction throughput (IPC in instructions/cycle) versus the superscalar factor (S) on a linear-linear scale (S is the X axis, IPC is the Y axis).

Part 1.B: Now add effects of mispredicted branches and repeat the plot.

Part 1.C: Based on this model, compute an “optimal” value of S (i.e., most reasonable balance of performance and efficiency). Defend your choice.

QUESTION TWO: (20 points) Using information found on the WWW, prepare a **one page** technical summary of *victim caches*. Explain how they work, who they are different that traditional caches, and what improvement they offer. Provide citations (with URLs) for all materials used in your study.

QUESTION THREE: (25 points) Provide a *concise* comparison of the dynamic instruction execution approach for the PPC604 and the UltraSPARC Ili. How are the two processors approach to maximizing instruction throughput different? Which architecture is more aggressive? Why?

QUESTION FOUR: (15 points) State three reasons (4.A-4.C) why a CISC instruction set architecture (e.g., i8086) would be difficult to implement using the baseline execution architecture define in class.