

PROJECT DESCRIPTION: In this project, you will write a trace driven execution simulator for a superscalar MIPS architecture. With this simulator, you'll explore the effect of *superscalar factor*, *reservation stations per function unit*, and *number of functional units* on execution time (measured in cycles).

SYSTEM DEFINITIONS: In addition to the execution constraints defined in the execution architecture description, the following characteristics can be assumed:

- Instruction fetches hit in the caches 98% of the time.
- Data fetches hit in the cache 95% of the time.
- All caches misses incur a 4 cycle delay.

The number of functional units is defined as the N copies of the four units described below. Assume that multiple instructions can be dispatched to reservation stations on a single functional unit in a cycle. All functional units are fully pipelined. A cycle is required to distribute results following the execution latency listed below. There are a total of six stages: fetch, decode, dispatch, execute, distribute, and commit. The following execution times apply to the functional units:

integer arithmetic	floating point arithmetic	memory accesses	branch computation
1 cycle	3 cycles	2 cycles	1 cycle

TRACE EXAMPLES: Two trace files are available from the class web site. (Caution: the files are large!). The files are in ASCII format with each entry containing the instruction address, instruction word, and assembly language source. The instruction word (broken into two parts) is the easiest to parse. The instructions are in MIPS format.

TRACE EXECUTION: While trace execution does not require actual execution of the instruction operations, the specific execution behavior can only be determined by performing accurate scheduling of instructions in the dispatch, execution, and commitment stages. The accurate simulation of the renaming and reorder buffer and reservation stations is necessary to achieve accurate execution cycle counts. Delays on loads, stores, and instruction fetches are determined probabilistically. Branches are to be through simulation of a 512-entry fully associative BTAC and 512 entry BHT. Assume both the BTAC and BHT are word (instruction) addressed. If a branch is determined to be mis-predicted, no further instructions are accesses from the trace until the branch completes execution in the branch functional unit.

METRICS: The principal performance metric is instructions/cycle throughput (IPC). However, large, complex execution hardware is slower yielding a longer cycle time. Assessments of performance should consider the implementation parameter's affect on cycle time and system cost. Measuring resource utilization (reservation stations, functional units, instructions dispatched per cycle) provides important insight into trace execution. Histograms are more useful than averages.

PROJECT REPORT: The project report is limited to ten pages, using a 12 point times roman font, 12 point spacing, and one inch margins on all sides. The report should be submitted in PDF format. The format of the report is as follows:

1. Title and Authors

2. Abstract (summarize reports conclusions in 100 words or less)
3. Introduction (state what is being studied, related work; briefly summarize results)
4. Experiment (describe simulation process, test data, validation of simulator)
5. Results and Analysis (show results obtained from simulator, analyze and explain results)
6. Conclusions (summarize critical results and impact on future architectures)