ECE 3055: Computer Architecture and Operating Systems

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Course Objectives

- Core concepts of microprocessor architecture
  - Instruction Set Architecture (built on ECE 2030 concepts)
  - ALU, Datapath, & Control Implementation
  - Pipelined datapath operation
  - Cache memory hierarchy
  - Virtual memory
  - Basic input/output systems
- Core concepts of operating systems
  - Processes/threads
  - Protection
  - Resource Management
  - Scheduling
  - File Systems

Course Objectives

- Understand how computing systems work
  - Fundamental concepts and key challenges
  - Understanding performance
- Acquire knowledge to optimize systems
  - As a designer
  - As a user
  - As a researcher
- Build simple processor models and apply several hardware optimizations
- Implement basic operating system primitives

Course Information

- Web page: http://www.ece.gatech.edu/academic/courses/summer2008/ece3055
  - Will be constantly updated, so check it regularly
- Prerequisite: ECE2031 Digital Design Lab
- Textbooks
  - Patterson and Hennessey, *Computer Organization & Design: The Hardware/Software Interface* (3rd edition), Morgan Kaufmann, 2007. ISBN 1-55860-604-1
  - Silberschatz, Galvin, and Gagne, *Operating System Concepts with Java* (7th edition), John Wiley, 2004. **ISBN-13:** 978-0471694663 .

Grading Policy

- 6 Programming Assignments: 30% (equally weighted)
  - Individual work, no collaboration
  - No late assignments will be accepted
- Exams
  - 2 in-class exams: 40% (20% each, dates TBD)
  - Final: 30%: August 1st, 2:50 pm – 5:40 pm
- Teaching Assistant: TBD

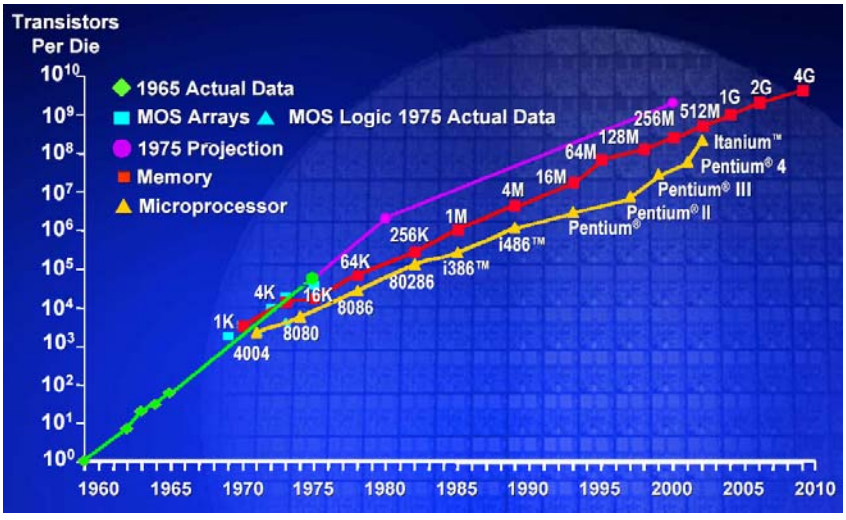
Introduction

Historical Perspective

- ENIAC built in World War II was the first general purpose computer
  - Used for computing artillery firing tables
  - 80 feet long by 8.5 feet high and several feet wide
  - Each of the twenty 10 digit registers was 2 feet long
  - Used 18,000 vacuum tubes
  - Performed 1900 additions per second

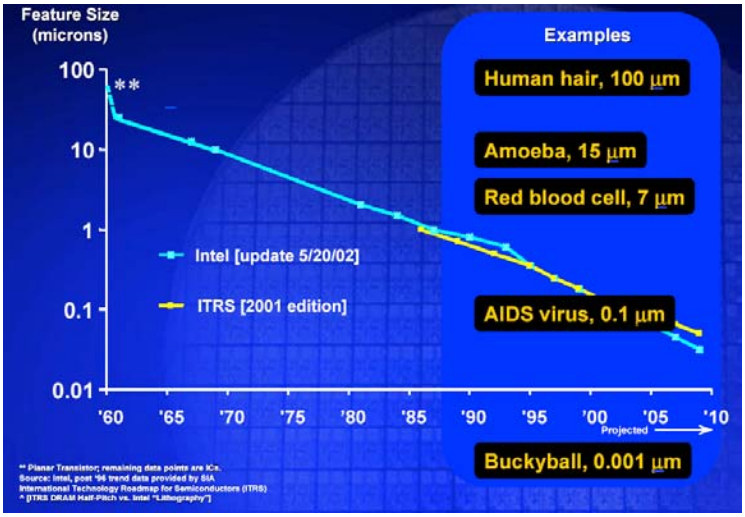
– **Since then Moore's Law**
  – **Transistor density doubles every 18-24 months**
– **Modern version**
  – **#cores double every 18-24 months**

Integrated Circuits Capacity



Source: Courtesy H.H. Lee, ECE 3055

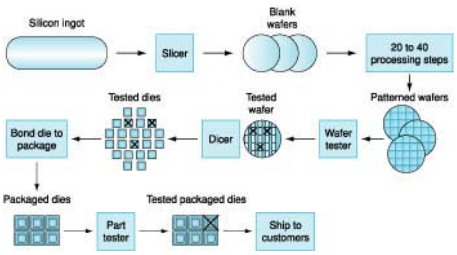
Feature Size

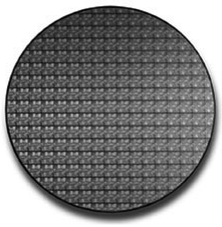


We are currently at 0.09µm and moving towards 0.065µm

Source: Courtesy H.H. Lee, ECE 3055

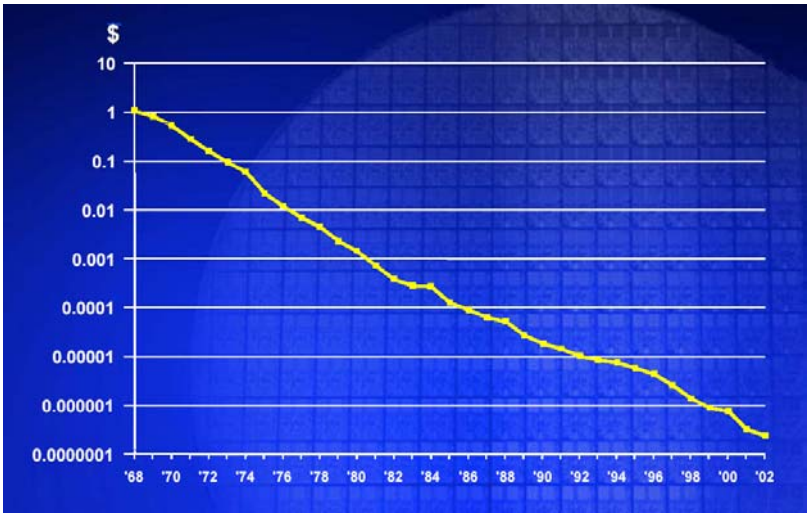
Understanding Cost





- What happens if you simply port a design across technology generations?

Average Transistor Cost Per Year



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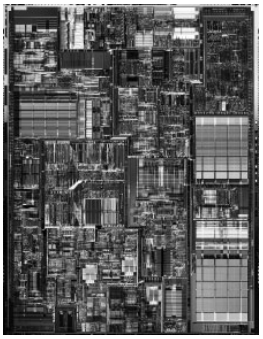
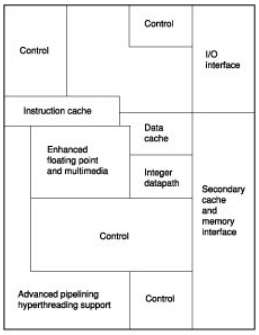
Pentium 4





- Note the area devoted to control!
  - Keep the functional units busy
- Note the area for the cache
  - Avoid going off chip

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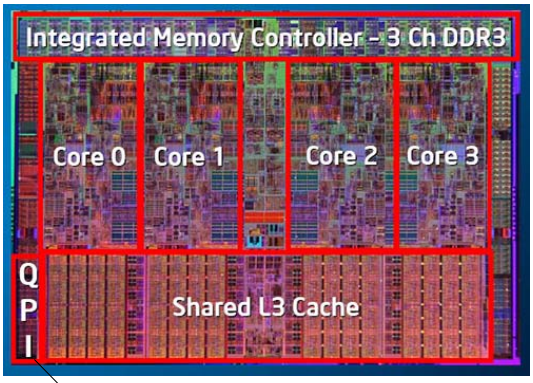
Advent of Multicore

- On chip memory controller

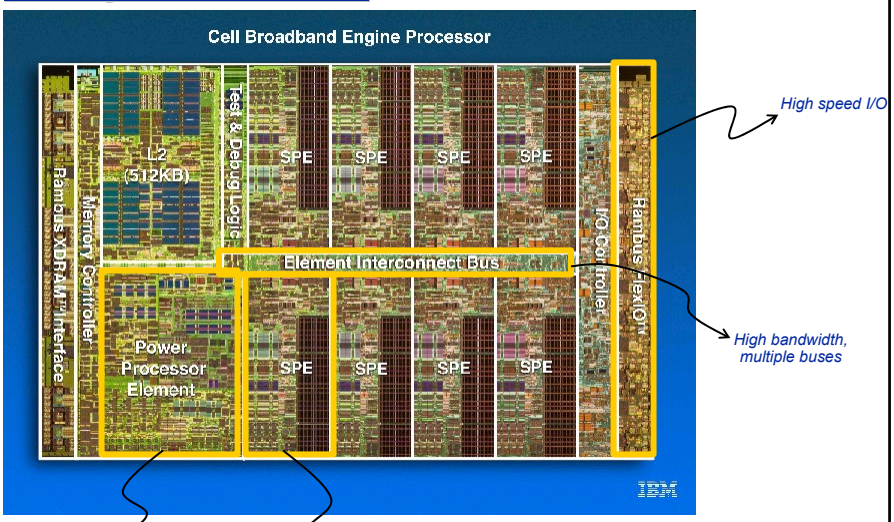


- 731M transistors
- 32Kbyte L1 I&D caches
- 256Kbyte L2/core
- 8MB shared L3

- Intel's next generation front side bus

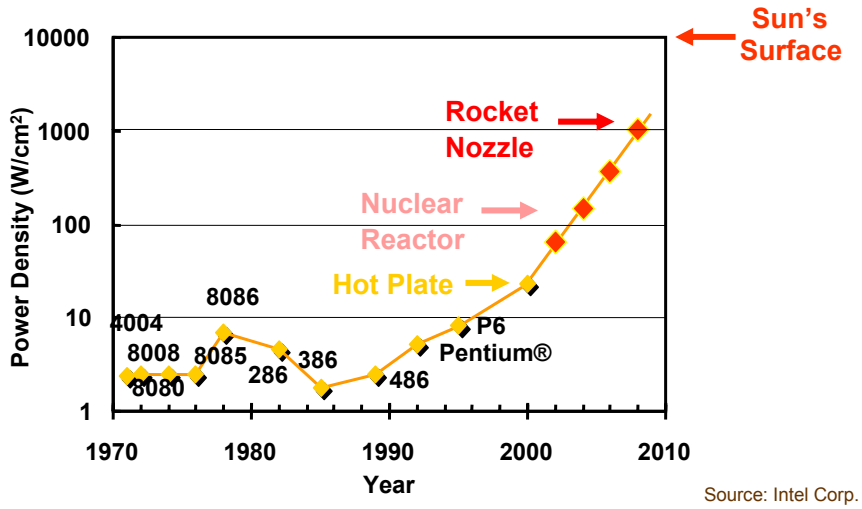
The Advent of Multi-Core

Heterogeneous MultiCore



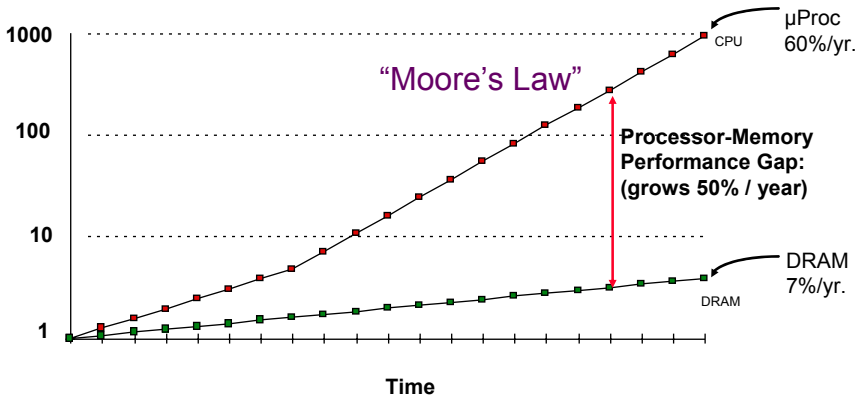
Source: IBM

The Power Wall



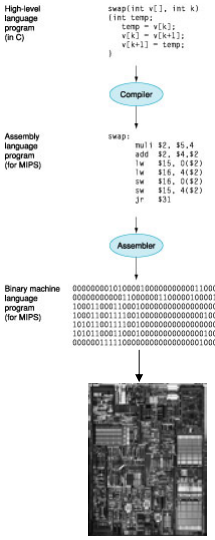
Source: Intel Corp.

The Memory Wall



Hierarchy and Abstraction

- *Performance is a function of both the compiler and the hardware!*
  - Language/Compiler/Architecture determine machine instructions (Chapter 2 and 3)
  - Processor/Memory determine how fast instructions are executed (Chapter 5, 6, and 7)

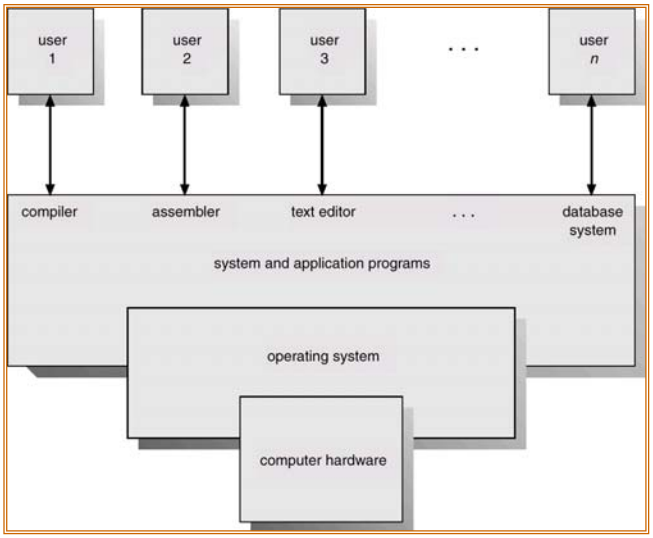


Instruction Set Architecture

- A very important abstraction
  - interface between hardware and low-level software
  - standardizes instructions, machine language bit patterns, etc.
  - advantage: *different implementations of the same architecture*
  - disadvantage: *sometimes prevents using new innovations*

- Modern instruction set architectures:
  - 80x86 (aka iA32), PowerPC (e.g. G4, G5)
  - Xscale, ARM, MIPS
  - Intel/HP EPIC (iA64), AMD64, Intel's EM64T, SPARC, HP PA-RISC, DEC/Compaq/HP Alpha

Software Abstractions and the Operating System



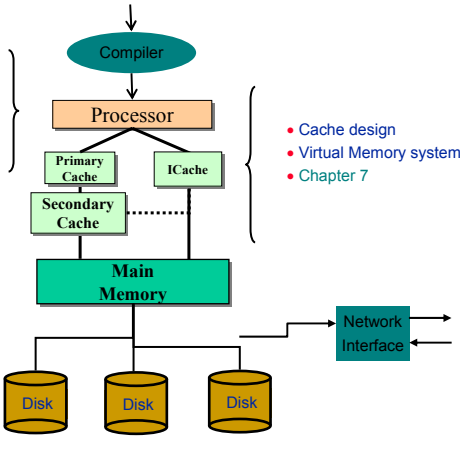
Source: Silberschatz, Galvin, and Gagne, *Operating System Concepts with Java* (7th edition),

Above the Hardware

- The operating system provides a civilized veneer on the raw hardware
- Provides for sharing of physical resources
  - Concurrency is central to operating system functionality
  - Synchronization is central to managing concurrency
  - Abstractions for capturing concurrency and synchronization
    - Threads, processes, semaphores, locks, etc.

Course Layout: Part I Computer Architecture

- Instruction set architecture
- ALU implementation
- Single & Multi-cycle datapath
- Pipelined Datapath
- Chapter 2, 3, 4, 5, 6



- Cache design
- Virtual Memory system
- Chapter 7

- Storage technologies
- I/O systems
- Chapter 8