Final Exam Study Guide

For all of the following modules, you should be familiar with and able to explain all of the terms in the glossary provided at the end of each module's power point presentation.

**Instruction Set Architecture**
- Be able to rearrange data in memory for common data structures to be able to get better cache behavior (using data directives). Why does this matter? Consider the layout of a matrix in memory.
- Synchronization support
  - Understand the implementation of the `load-linked` and `store-conditional` instructions in the MIPS ISA for implementing synchronization operations.
- Understand MIPS procedure call conventions
  - Call-return address linkage

**Arithmetic**
- Understand the basic energy/power behavior of an ALU
  - What are the sources of energy dissipation?
  - Understand the difference between power and energy

**Pipelined Datapath and Performance**
- Hazards:
  - Data hazards, structural hazards and control hazards
  - Be able to distinguish between them and be able to identify all hazards in a sequence of SPIM code
- Schedule code
  - To avoid or minimize pipeline stalls
- Modify the pipeline and control to be able to add new instructions
- Show the sequence of instructions that flow through the pipeline on a page fault
- Compute the number of cycles to execute a code block given a pipeline and an integrated I-cache and D-cache.
  - Given instruction statistics as well as the probabilities of various hazards, compute the CPI and execution time including cache effects, e.g., miss rates.
  - Re-computation of the CPI when the pipeline is modified
- Be able to apply Amdahl’s Law to simple cases.
- Update the datapath to include a I-cache, D-cache, TLB or TLBs, i.e., where will they be placed and how will they be referenced.
- Update the datapath to be able to execute multiple threads.

**Memory and Virtual Memory**
- Describe (with examples) spatial and temporal locality
- Describe how a set associative cache works, and by extension fully associative and direct mapped caches
- Address breakdown for all caches in a multilevel cache hierarchy
• DRAM organization and computation of miss penalties
• Computation of the impact of cache misses on CPI
• Multilevel cache organization and operation
• Write-through vs. writeback design – how are they different and how does each one impact the CPI?
• Apply an address sequence to a multilevel cache hierarchy
• Compute the size of the page table
• Operation of the TLB on a miss
  o When the referenced page is in memory
  o When the referenced page is not in memory
• On a memory reference, understand the operation of the complete memory hierarchy – from TLB down to DRAM through a multilevel cache hierarchy. Updating the data structures.
• The ability to update cache directories for implementing a simple invalidation based coherence protocol.
• Relationship between pages and cache lines.

**Parallelism**
Demonstrate an understanding of the following concepts in terms of being able to describe them, or distinguish between them.

• ILP, TLP, and DLP
• SIMD vs. MIMD vs. Vector
• Forms of multithreading: fine grained and coarse grained
  o Show an example of each type of threading