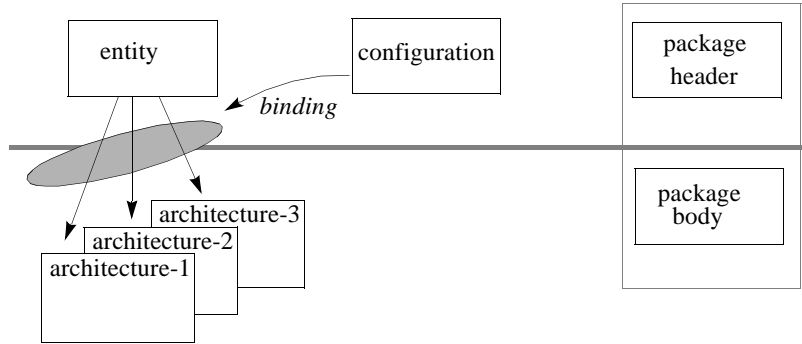


## Programming Mechanics

- Basic unit of VHDL programming is a design unit which is one of the following

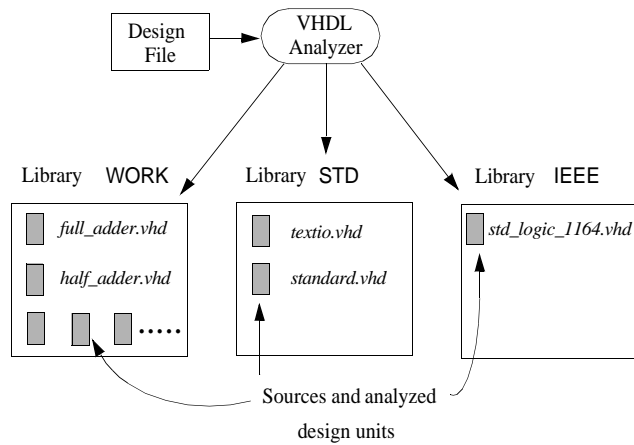
*Primary Design Units*



*Secondary Design Units*

1

## Compilation, Naming and Linking



- Design unit names are used to construct intermediate file names
- The libraries WORK and STD

2

## Basic Steps: Simulation

- Analysis and Analysis (Compilation) Order
  - primary vs. secondary design units
  - organization of design units and files

**architecture** structural of full\_adder is

**component** half\_adder is

**port** (a, b : in std\_logic;

sum, carry : out std\_logic);

**end component** half\_adder;

**component** or\_2 is

**port** (a, b : in std\_logic;

c : out std\_logic);

**end component** or\_2;

**signal** s1, s2, s3 : std\_logic;

**begin**

H1: half\_adder **port map** (a => In1, b => In2, sum => s1, carry=> s3);

H2: half\_adder **port map** (a => s1, b => c\_in, sum => sum, carry => s2);

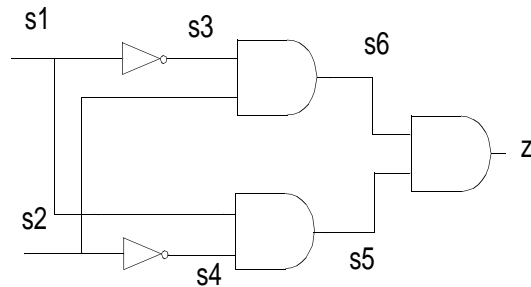
O1: or\_2 **port map** (a => s2, b => s3, c => c\_out);

**end architecture** structural;

3

## Basic Steps: Simulation

- Elaboration
  - of the hierarchy produces a netlist of processes



- of generics
- storage allocation
- initialization

4

## **Basic Steps: Simulation**

- Initialization
  - all processes are executed until suspended
  - initialize simulation time
- Simulation
  - discrete event simulation
  - two step model of time
    - set net values
    - execute all affected processes and schedule new values for nets
  - simulator step time