State of the art supercomputers rely on the interconnection of hundreds to thousands of high speed processors. Research and development of necessary interconnection networks have progressed triggered by new technologies and demands and are distinct from local and wide area communication networks. The advent of the multi-core and many-core designs signals a transition to on-chip interconnection networks. This course covers the design and analysis of multi-processor & multi-core networks. The course covers the fundamental theory encompassing deadlock and live-lock freedom of routing protocols, congestion management, and performance modeling. This material is vertically integrated relating the theory to aspects of the design of high speed routers, flow control protocols, and routing algorithms and the distinguishing features of on-chip and off-chip network designs. Finally we will present case studies covering modern commercial examples. Laboratory exercises will involve simulation of network architectures, routing protocols, and the evaluation of design trade-offs.


Topical Outline

Network Topologies
- Direct Networks
- Switch-Based Networks
- Crossbar and Bus Networks

Switching Techniques
- Circuit, Packet, and Wormhole Switching
- Virtual Channels
- Hybrid Switching Techniques such as PCS, and Buffered Wormhole.
- Comparison of Switching Techniques

Deadlock, Livelock, and Starvation
- Theory of Deadlock Avoidance
- Deadlock Recovery Mechanisms

Routing Algorithms
- Oblivious and Adaptive Routing
- Multicast Routing
- Fault Tolerant and Reliable Routing
Router Architecture
    Design of oblivious and adaptive routers
    Cost/Speed Model for router architectures
    Overview of commercial routers from the Blue Gene, Alpha, Cray T3D,
    Black Widow, and emerging on-chip networks such as Philips,
    Fulcrum, and ST MIcroelectronics
    Hardware support for multicast, fault tolerance, and deadlock recovery
    High Radix switch designs

Messaging Layer Implementation
    Network Interface Architecture
    User Level Messaging and Buffer Management

Network Optimization
    Physical constraints and network scaling
    Optimizing network topology and channel operation
    Power efficient network design

Emerging Trends and Open problems
    On-chip interconnection networks (OCINS)
    Case studies of OCINs

Course Grading:
Mid-term: 20%
Assignments: 30%
Research Project (Report and Presentation): 50%

The early part of the course will cover the underlying theory which has been developed in
the last 12 years. The midterm will test knowledge of this theory. The remainder of the
course will follow a research format. The assignments will introduce the students to the
analysis and simulation tools. The research project will cover a research problem in
modern interconnection networks. Students will study relevant papers, propose a
solution, implement the solution (simulation or FPGAs), document the project (short
paper) and present the paper in a conference format (20 minutes).