

ECE 3042

Fall 2009 Homework Problem Set 7 for Experiment No. 9

Due Week of October 26

1. Design a 555 timer circuit to produce a TTL clock signal with a duty cycle of 55% and a frequency of 66 kHz. This entails determining suitable values for the components in Fig. 9-10, viz R_1 , R_2 , and C_T . The maximum value of the sum of the two resistors should be less than 3 M Ω . Also neither resistor should be less than 900 Ω . The capacitor should be larger than 500 pF. Pick standard components so that this circuit can be implemented in lab. Because this is to be a clock signal for a TTL logic system the dc power supply $V_{CC} = 5$ V. (The 555 is a favorite of hobbyist. A web tutorial can be found at <http://www.uoguelph.ca/~antoon/gadgets/555/555.html>)

Verify the design of the 555 timer circuit by performing a National Instruments (Multisim) SPICE simulation of the circuit. Perform a transient analysis that will display at least 5 cycles of the output. Plot the output TTL clock voltage and the threshold voltage (capacitor voltage) as functions of time. (Be certain to set the initial value of the capacitor voltage to zero.)

2. Determine the resistors R_A and R_B required for the D/A circuit to produce a zero code voltage of -12 V, $V_z = -12$ V, and an all ones voltage of $V_1 = 12$ V. Perform the calculation for both the 4 and 8 bit systems that will be implemented in lab. Determine the range voltage for the 4 and 8 bit systems. Determine the resolution voltage.