

ECE 3042

Fall 2009

Homework Set No. 8 for Experiment No. 16

Due Week of November 16

1. Design a common source single stage MOSFET amplifier circuit (Fig. 16-12) to have a small-signal gain with a magnitude of 5. Bias the circuit so that the dc drain current is 1.2 mA. The small-signal input impedance is specified to be 150 k Ω and the small signal output impedance is 10 k Ω . The load resistor is 20 k Ω . The dc power supply voltages are $V^+ = +15$ V and $V^- = -15$ V. The parameters of the transistor are: $K = 278 \mu\text{A}/\text{V}^2$, $V_{TO} = 1.606$ V, $C_{GDO} = 2.5$ nF/m, $C_{GSO} = 2.5$ nF/m, and $\lambda = 0.014$ V $^{-1}$. Pick $C_1 = C_2 = 0.22 \mu\text{F}$, and $C_3 = 10 \mu\text{F}$.

Verify the design with a either a Cadence and National Instruments SPICE analysis. Use a DC analysis to determine the bias. Use an AC analysis to plot the gain versus the frequency. Choose the lower frequency as 1 Hz and the upper frequency 10 GHz. Mark the midband gain and the -3 dB frequencies. The SPICE parameters are KP ($2K$), VTO (V_{TO}), LAMBDA (λ), CGDO (C_{GDO}), and CGSO (C_{GSO}). If the version of SPICE used requires the width (W) and length (L) of the channel use 10 μm for each. Perform a transient analysis to determine the upper and lower clipping levels.

Compare the lower -3 dB frequency with that predicted by Eqn.16-46.