ECE 4043
Spring 2020

Homework for 7 for Experiment No. 7

Due Week of March 2

1. Shown below is a single stage common source amplifier biased by a current mirror current source. Bias the circuit so that the dc drain current is $1.86\,\mathrm{mA}$,viz pick R_T so that the drain current in each transistor has this value. The small-signal input impedance is specified to be $50\,\mathrm{k\Omega}$ and the small signal output impedance is $5.1\,\mathrm{k\Omega}$ (Assume $\lambda = 0$ for this specifications). The load resistor is $10\,\mathrm{k\Omega}$. The dc power supply voltages are $V^+ = +15\,\mathrm{V}$ and $V^- = -15\,\mathrm{V}$. The parameters of the each transistor are: $K = 1\,\mathrm{mA/V^2}$, $V_{TO} = 1\,\mathrm{V}$, $\lambda = 0.001\,\mathrm{V^{-1}}$, $C_{GDO} = 2.5\,\mathrm{nF/m}$, and $C_{GSO} = 2.5\,\mathrm{nF/m}$. Pick $C_1 = C_2 = 22\,\mu\mathrm{F}$, and $C_3 = 330\,\mu\mathrm{F}$.

Verify the design with a SPICE analysis using National Instruments SPICE Multisim .

For the SPICE analysis use a DC analysis to determine the bias. Use an AC analysis to plot the gain versus the frequency. Choose the lower frequency as $1\,\mathrm{Hz}$ and the upper frequency $10\,\mathrm{GHz}$. Mark the midband gain and the -3 dB frequencies. The SPICE parameters are `KP` $(2K)$, `VTO` (V_{TO}), `LAMBDA` (λ), `CGDO` (C_{GDO}), and `CGSO` (C_{GSO}). If the version of SPICE used requires the width (W) and length (L) of the channel use $10\,\mu\mathrm{m}$ for each. Perform a transient analysis to determine the upper and lower clipping levels. (Remember the SPICE parameter $KP = 2K$.)