Georgia Institute of Technology
School of Electrical and Computer Engineering
ECE 4435 Op Amp Design Laboratory Fall 2003

Design Project 2
An Automatic Noise Gate

Introduction.

Noise in audio recording and transmission systems is an ever present problem. The background noise in the audio track of old movies shown on TV is a familiar example. Other examples are noise in magnetic tape recordings, public address systems, broadcast studios, studio-to-transmitter links, telephone lines, etc. In most cases, most of the power in the background noise is at high frequencies. It follows that the noise can be removed if the signal is passed through a low-pass filter. However, the filter will also filter out the desired high frequencies in the signal. A solution that has been used to solve this problem is a low-pass filter that is controlled by the signal. Such a device is also called a noise gate. If the high-frequency content of the signal is small, the bandwidth of the low-pass filter is reduced. If the high-frequency content of the signal exceeds some manually adjustable threshold, the filter bandwidth increases so that the full bandwidth of the signal is passed. Although the noise is passed also, the signal masks the noise so that it is not objectionable. When the high-frequency content of the signal drops below the threshold, the bandwidth of the filter again decreases so that the noise is not passed.

Annoying audible effects are often produced because the gain change when the desired audio signal starts and stops can be audible. For example, the beginning of a word in speech can be lost if the attack gain change is not fast enough. Similarly, low level instruments in music can be lost if the noise gate threshold is too high. The object of this design project is to design a noise gate which reduces the audible effects by changing the gain of only the high-frequency portion of the signal so that only the undesirable hiss is removed. The gain change is to be as "smooth" as possible to minimize undesirable audible effects.

Circuit Specifications

1. There will be one unbalanced input and one unbalanced output.

2. When the bandwidth of the noise gate is a maximum, the midband voltage gain from the input to the output is to be unity ± 0.1 dB when measured at an input level of 1 V rms.

3. The circuit must be capable of driving a $600\,\Omega$ load at its output to a level of +6 dB above 1 V rms with a sine wave input signal in the frequency range of 20 Hz to 20 kHz with an overload margin before clipping of +6 dB or more.

4. At a test frequency of 1 kHz, the total harmonic distortion in the output signal must not exceed 0.5% at the rated output level.

5. When the bandwidth of the noise gate is a maximum, the lower -3 dB cutoff frequency must be $10\,\text{Hz} \pm 5\%$ when measured at an input level of 1 V rms. The upper -3 dB cutoff frequency must be 30 kHz or greater.

6. This specification describes the operation of the noise gate in varying the bandwidth of the circuit. The buffered audio input signal is to be filtered with a unity-gain, single-pole, high-pass filter having a time constant of $75\,\mu$s. The output of this filter is to be full-wave rectified and detected by a peak detector circuit. The peak detector should not have any saturating op

amps. The peak detector is to have a release time constant of 200 ms. The output of the peak detector is to be used to control the bandwidth of the overall circuit. With no input signal, the output of the peak detector is zero and the overall bandwidth is to be that of a single-pole, low-pass filter having a time constant of 75 μs. When the output from the peak detector increases from 0 V, the bandwidth is to increase to 30 kHz or greater. A potentiometer is to be used to control the signal input to the peak detector so that the input level to the overall circuit at which the bandwidth is 30 kHz can be adjusted between 0.1 V rms and 1 V rms.

7. The dc offset voltage at the output must have a magnitude less than 50 mV.

8. The output impedance must be $100\,\Omega \pm 10\%$.

9. The input impedance must be $20\,\text{k}\Omega \pm 10\%$.

Some special purpose circuits which you may consider using in the design are band splitters, precision rectifiers, peak detectors, and a JFET operated as a variable resistor. A method for doing the latter will be covered in class.

Design Considerations.

An important criterion of your design will be the correlation you can achieve between your experimental laboratory results, SPICE computer simulations, and your theoretical calculations. In your preliminary design, you can consider all operational amplifiers to be ideal. Your final design circuit should be capable of being tuned to compensate for non-ideal characteristics occurring in op amps and other components. Keep in mind that you should be designing a circuit which can be mass produced and widely utilized. Therefore, it should be easily adjusted with off-the-shelf components.

Comparisons should be made among the response of an ideal noise-gate circuit, the theoretical circuit response as predicted by SPICE, and the experimental circuit response. In the lab, it will be relatively easy to measure a frequency response characteristic using the laboratory equipment. Comparing theoretical, experimental, and SPICE transfer characteristics will be essential in checking the quality of your design.

Power supplies of ± 15 V and $+5$ V are available for your design.

Design Schedule

1. Submit for approval a preliminary "paper design" to your lab GTA for his review on or before class September 29, 2003. This paper design should show a possible block diagram with complete circuit diagrams of each block with all component values chosen. Also, provide design equations and explain the thought processes behind your preliminary design. This preliminary design does not have to be the final design you realize for this experiment, but it should help you begin to solidify the underlying concepts and specifications. Remember, the more information that you can provide for your lab GTA, the more direction he can give you and the more time he can save you in the laboratory. Your "paper design" should be complete enough so that you can begin to assemble and test your design in your laboratory period during the week of September 29.

2. Utilize SPICE to theoretically verify your circuit design. Use the 741 or LF351 op-amp macromodels that are given on page 35 of the document located on the class web page at http://users.ece.gatech.edu/~mleach/ece4435/chap02.pdf. Obtain SPICE transfer characteristic plots for the output. Present this SPICE verification of your design to your lab GTA for his certification at your regular lab period during the week of October 6.

3. Complete the laboratory evaluation of your design with a witness verification of proper design performance during lab the week of October 13.

4. Submit your complete report to your lab GTA during lab the week of October 20.

References

Some useful references for the design can be found in Chapters 3 and 9 of the text and in chapters 5 and 14 of the ECE 3042 Lab Manual. You are encouraged to use utilize the library for further references.

Design Evaluation Criteria

1. Design approach, philosophy, and clarity of explanation. Follow suggestions given in the "Op Amp Design Lab Procedures and Instructions" sheet on the class web page.

2. Achievement of design specifications.

3. Documentation of design performance.

4. Design simplicity and economics. Evaluate the cost of your design according to the instructions on the "Op Amp Design Lab Procedures and Instructions" sheet.

5. Assume that your design is to be used in an application requiring large quantity production using off-the-shelf components.

6. Other Components: If you are considering using some special device or component, determine the cost and availability of a tested and guaranteed unit from a reliable vendor. With this information, your laboratory GTA will determine the equivalent cost units.

ECE 4435 Design Project Evaluation Criteria

Prelab Submitted on 09/29/03	5 points
Laboratory Attendance	10 points
Explanation of Design Approach & Insight Into Design	10 points
Block Diagram of Circuit	
Derivation of Gains and/or Transfer Functions	
Design of the Full-Wave Rectifier and Peak Detector	
Design of the High-Frequency Noise Gate Circuit	
Derivation of Half-Power Frequencies	
Input Impedance Considerations	
Output Impedance Considerations	
Results & Presentation of SPICE Simulations	5 points
"Signed Off" in Lab during the second lab period	
SPICE Simulation of Final Overall Circuit	
Presentation	
Economics & Cost Analysis	5 points
Justify Design Choices	
Total Component Cost	
Presentation of Experimental Results	5 points
Complete Documentation of Results Verified in Lab	
Comparison of Theoretical, SPICE, and Experimental Results (In Tabular Form with % Errors)	
Explanation of Results	
Explanation of Measurement Techniques	
Experimental Results Obtained	5 points
Gains	

Half-Power Frequencies
Frequency Response of Noise-Gate Circuit
Operation of Full-Wave Rectifier
Operation of Peak Detector Circuit
Manually Adjustment of Control Range
Input & Output Impedances
Overload Margin
Output Offsets

Conclusions 5 points

Sources of Error
Proposed Improvements to Circuit
General Comments on Whether Specifications are Reasonable
General Comments on Whether Measuring Techniques are Reasonable

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Evaluation Sheet for Design Project 2
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Name:_____

_____ 05 Verification of Preliminary Design
_____ 10 Laboratory Attendance
_____ 05 Explanation of Design Approach
_____ 05 Demonstration of Insight into the Design
_____ 05 Results and Presentation of SPICE Simulations
_____ 05 Economics and Cost Analysis
_____ 05 Presentation of Experimental Results
_____ 05 Experimental Results Obtained
_____ 05 Conclusions
_____ 50 Total

Verification of Experimental Results

Parameter	Specification	Result	Witness
Midband Gain	unity $\pm 0.1\,\mathrm{dB}$		
Frequency Response Above Threshold	$10\,\mathrm{Hz}$ to $\geq 30\,\mathrm{kHz}$		
Input Resistance	$20\,\mathrm{k}\Omega \pm 10\%$		
Output Resistance	$100\,\Omega \pm 10\%$		
HP and LP Pole Time Constants	$75\,\mu\mathrm{s}$		
Peak Detector Release Time Constant	$200\,\mathrm{ms}$		
Level Adjustment for Full Bandwidth	$0.1\,\mathrm{V}$ to $1.0\,\mathrm{V}$ rms		
THD	$\leq 0.5\%$		
Output Level into $600\,\Omega$	$+6\,\mathrm{dB}$ over $1\,\mathrm{V}$ rms		
Overload Margin	$+6\,\mathrm{dB}$		
Output DC Offset	$< 50\,\mathrm{mV}$		

Witnessed by: _____ Date: _____