An Inductorless Wideband Balun-LNA in 65nm CMOS with balanced output

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***Abstract* — An inductorless LNA with active balun is designed for multi-standard radio applications between 100MHz and 6GHz. It exploits a combination of a common gate stage and a common source stage with replica biasing to maximize balanced operation. The NF is designed to be around 3dB by using the noise canceling technique. Its best performance is achieved between 300MHz to 3.5GHz with gain and phase errors below 0.3dB and ±2degrees, 15dB gain, S11<-14dB, IIP3 = 0dBm and IIP2 higher than +20dBm at a total power consumption of 21mW. The circuit is fabricated in a baseline 65nm CMOS process, with an active area of only 0.01mm^2. The circuit simultaneously achieves impedance matching, noise canceling and a well balanced output.**

I. Introduction

Upcoming software-defined and multi-standard radio architectures demand wideband LNAs [1]. In contrast to a multi-LNA solution, a wideband LNA is flexible and efficient in terms of area, power and costs. Single-ended input LNAs are preferred to save I/O pins and because antennas and RF filters usually produce single ended signals. On the other hand, differential signaling in the receive chain is preferred in order to reduce second order distortion and to reject power supply and substrate noise. Thus, at some point in the receive chain a balun is needed to convert the single-ended RF signal into a differential signal. Off-chip baluns with low losses are typically narrowband so that several baluns would be required in case of wideband operation. On the other hand, wideband passive baluns typically have high loss, degrading the overall NF of a receiver significantly.

Combining the balun and LNA functionality into a single integrated circuit is an attractive option to realize a wideband low noise receiver front-end. Only a few wideband LNA-balun combinations with sufficient low noise figure for multi-band receivers have been published [1-3]. These circuits all exploit the noise canceling topology published in [4, Fig. 4b]. Although these circuits have a single-ended input and differential ouput, the (im)balance of the output signal is not reported. Furthermore, the circuit in [1, Fig. 8a] inherently has a gain difference between its two paths, leading to an unbalanced output signal. Both paths use an equal load resistor (R_L), however, the transconductance (g_m) differs more than a factor of 2, leading to a gain difference ($\Delta g_m \cdot R_L$) of at least 6dB. Next to this, the circuits in [1-3] all use integrated inductors. As in newer CMOS technologies the area-costs increase, area-consuming integrated inductors become increasingly expensive. Thus, for CMOS processes an inductorless implementation is strongly preferred.

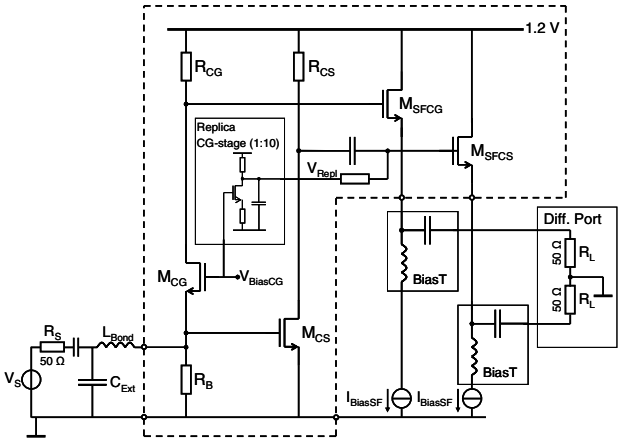

Figure 1. Schematic of the Inductorless Wideband Balun-LNA; the circuit within dashed box is integrated on chip.

This paper presents an inductorless Balun-LNA with a well balanced output signal. The wideband circuit is designed in a baseline 65nm CMOS process with a 1.2V supply voltage, aiming for high linearity. The circuit is described in section II. Section III describes that noise canceling of the input transistor noise and a balanced output signal can be obtained simultaneously, using the Noise Canceling Technique. Section IV gives the measurement results. Finally the conclusions are drawn in Section V.

II. Circuit Description

Fig. 1 shows the balun-LNA circuit based on the topology proposed, but not implemented on silicon, in [4]. The circuit inside the dashed box is implemented on silicon. The input signal is amplified via two paths, a non-inverting Common Gate (CG) path and an inverting Common Source (CS) path. The voltage gains of these two paths are designed to be equal, giving the balun function. The outputs of both amplifier paths are buffered by identical source-followers, both having 50Ω output impedance. The source-followers are currently used as measurement buffers; in a complete receiver design they can drive a mixer. To maximize balanced operation, the DC-levels

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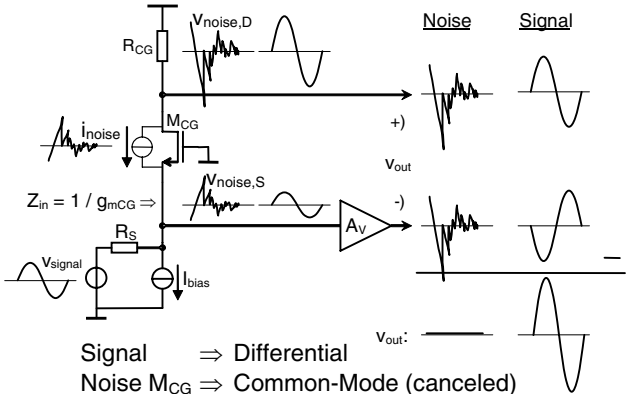

Figure 2. The Noise Canceling Technique applied to a CG-stage.

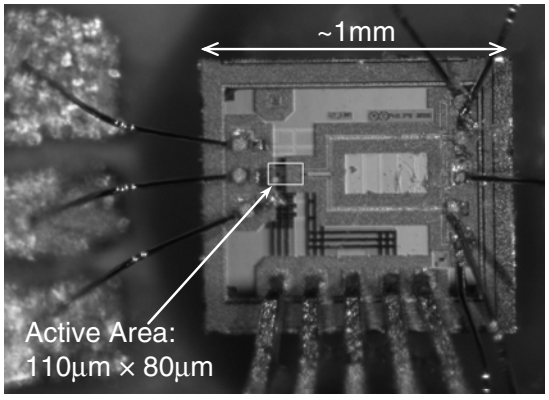

Figure 3. Die photo of the bonded Wideband Balun-LNA.

at the gates of the source followers are chosen equal. This is achieved by AC-coupling the output of the CS-stage to its source-follower and generating the DC-level (V_{Repl}) by a scaled-replica of the CG-stage. The cut-off frequency of the AC-coupling is designed to be at 10MHz. This is more than a decade below the intended operation frequency, which keeps the error in phase difference of the two paths within a few degrees of 180º.

The CG-stage inherently gives a broadband input match. The real part of the input impedance of the LNA is mainly set by $1/g_{mCG}$ of transistor M_{CG} in parallel with resistor R_B. When the input impedance is matched to the source impedance ($g_{mCG} \approx 1/R_S$, for $R_B >> R_S$), the noise of M_{CG} is the dominant factor in NF. Without taking any measures its noise would set the lower limit of the Noise Figure (NF) to ~4dB. However, by applying the Noise Canceling Technique [4], the noise of the CG-transistor can be canceled at the differential output. This Noise Canceling Technique is explained briefly in the next section.

Since the noise of M_{CG} can be canceled, the noise of M_{CS} remains. However, here the transconductance (g_{mCS}) can be chosen larger than $1/R_S$ while the input match is still performed by M_{CG}. The transconductance of M_{CS} (g_{mCS}) is chosen 5 times higher than g_{mCG} to limit its noise contribution. The resistor R_B acts as a current source and is chosen 7 times higher than R_S, thereby limiting its noise contribution.

III. Simultaneous Noise Canceling and Balancing

In this paper we dimension the CG-CS topology in such a way that simultaneous impedance matching, noise canceling and a balanced output signal are obtained. A balanced output requires the gains of the two paths to be equal.

Fig. 2 shows a simplified schematic of the circuit. The voltage amplifier (A_V) represents the CS-stage (M_{CS} and R_{CS}) of Fig. 1 and R_B is replaced by an ideal current source (I_{bias}). The noise generated by M_{CG} can be represented by a current source (i_{noise}). This current generates a voltage at the source-node of M_{CG} ($v_{S,noise}=\alpha \cdot i_{noise} \cdot R_S$) and a fully correlated voltage at its drain ($v_{D,noise}=-\alpha \cdot i_{noise} \cdot R_{CG}$) in anti-phase. The factor α depends on the CG-transconductance (g_{mCG}) and R_S: $\alpha = 1 / (1+g_{mCG} \cdot R_S)$. The noise of M_{CG} can be canceled when it becomes a common-mode signal at the differential output (v_{out}). Therefore, the gain of the CS-stage should be equal to: $A_V = v_{D,noise} / v_{S,noise} = -R_{CG} / R_S$. In order to match to the source impedance, the CG-transconductance should be equal to: $g_{mCG} = 1/R_S$. The required gain of the CS-stage can be rewritten as: $A_V = -g_{mCG} \cdot R_{CG}$, this equals the gain of the CG-stage, except for the inversion. Thus, at the output (v_{out}), the signal is fully differential (well balanced) and the noise of M_{CG} is common-mode signal, which is canceled when taking the differential output.

IV. Measurements

The LNA, which has an active area of only 110µm × 80µm, has been fabricated in a baseline 65nm CMOS process and is mounted on a PCB. The in- and outputs are bonded, the supply and bias are applied using a probe, see Fig. 3.

A. Gain, Input-match and Isolation

Fig. 4 shows the measured single-ended input to differential output S-parameter gain, S_{ds21}. This parameter characterizes the gain of the LNA using a 50Ω single-ended input port and a 100Ω differential output port. In practical use, the LNA will usually be followed by an on-chip mixer with a voltage-type input, and matching to 50Ω at the outputs is not needed. The most meaningful gain parameter is then the (unloaded) voltage gain. To convert S_{ds21} into voltage gain, 6dB needs to be added to account for the voltage-halving at the matched output, and an additional 3dB to take the conversion from 50Ω input to 100Ω output into account. Thus, the voltage gain is within 15.1dB ± 0.5dB from 100MHz up to 2.5GHz. The 3dB bandwidth is 5.2GHz. Fig. 4 shows that S_{11} is below -10dB up to 6.2GHz. The resonance of the input bondwire inductance (~1nH) and an external capacitor (600fF) broadens the input match with a few GHz.

The common and differential output to single-ended input isolations (S_{sc12} and S_{sd12}) are better than -30dB and -40dB respectively.

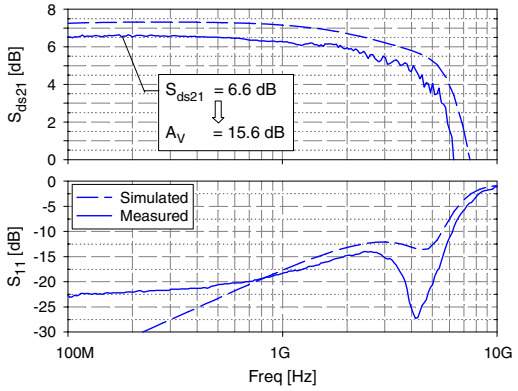

Figure 4. Simulated and measured S-parameters, S_{ds21} (Gain: single-ended in, differential out) and S_{11}

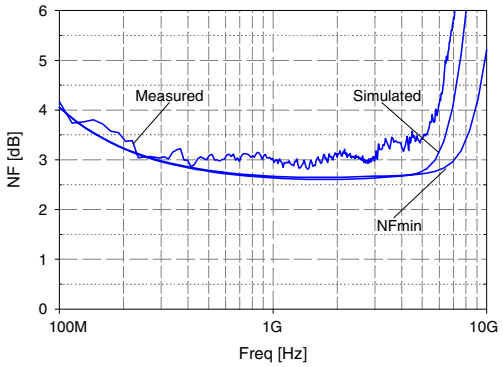

Figure 5. Measured Noise Figure, simulated NF and NF_{min}.

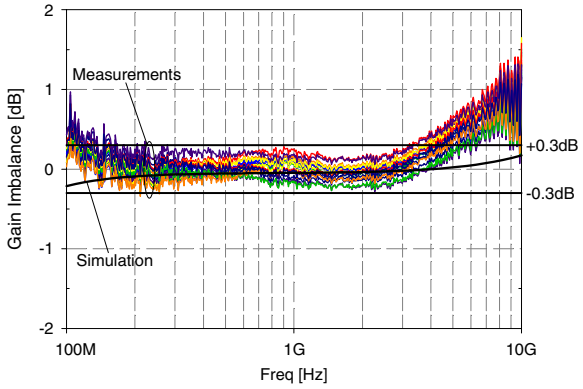

Figure 6. Gain imbalance, simulated and measured (20 samples).

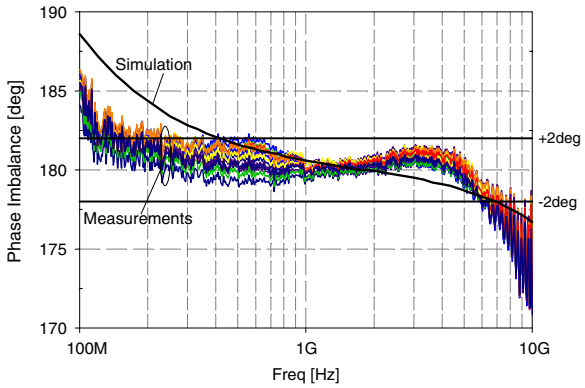

Figure 7. Phase imbalance, simulated and measured (20 samples).

B. Noise Figure

Fig. 5 shows that the measured Noise Figure (NF) is below 3.5dB from 0.2 to 5.2GHz and below 4dB from 0.1 to 6GHz. An advantageous property of the Noise Canceling technique is that the power and noise matching can be obtained simultaneously [4]. The simulated NF equals the simulated NF_{min} over a large bandwidth and only starts to deviate at higher frequencies due to the increasing impedance mismatch at the input. The increase of NF_{min} at low frequencies is due to 1/f-noise, the increase at high frequencies is due to the drop in gain.

C. Gain and Phase Imbalance

The balun performance was characterized on 20 samples at nominal bias conditions, equal to the simulation conditions. These measurements were preformed using wafer-probing. The gain and phase imbalance measurements are shown in Fig. 6 and Fig. 7. In the band from 300MHz to 3.5GHz the gain imbalance is smaller than ±0.3dB and the phase imbalance remains within ±2degrees. The somewhat larger spread in phase difference in the 300–800MHz range is caused by a resonance-effect in the output cables and non-optimal probe contacting. If desired, fine tuning of the balun functionality is possible, e.g. via the bias of the CS or GS stage or via the bulk of the CG transistor.

D. Linearity

Wideband standards like WiMedia-UWB and DVB-H require wideband RF-frontends with high linearity. For 2nd order distortion, a narrowband receiver is only sensitive to the effects of an interfering modulated carrier which leaks trough the mixer, corrupting the signal at the mixer output. Next to this effect, a wideband receiver also has to deal with interferers that have sum or difference frequencies equal to the wanted signal frequency, corrupting the signal already in the LNA. Analysis of interferer scenarios for two wideband standards, WiMedia-UWB and DVB-H, show that the required IIP2 of the LNA is around +20dBm.

Fig. 8 plots the 2nd order and 3rd order intercept points versus the frequency of one of the intermodulation tones. To determine the IIP2, one fixed 900MHz tone (e.g. GSM) is used, whereas another input tone is swept in frequency. For intermodulation frequencies below 900MHz the difference frequency is taken, for frequencies above 900MHz the sum frequency is taken as the intermodulation frequency.

The IIP3 is determined using two closely spaced tones and is around 0dBm. The increase in IIP3 with frequency can be explained by the increasing impedance mismatch at the input.

TABLE I. COMPARISON OF BALUN-LNAS, PASSIVE BALUNS AND INDUCTORLESS SINGLE-ENDED LNAS.

Ref	Freq. Band [GHz]	NF [dB]	Gain A_V [dB]	IIP2 [dBm]	IIP3 [dBm]	Pdiss (core) [mW]	Proc.[2] V_{supply}	# coils area [mm^2]	Balun?	Gain imbal. [dB]	Phase imbal. [deg]
This Work	0.2 – 5.2	< 3.5	13 – 15.6	**> +20**	> 0	21 (14)	65nm 1.2V	**– 0.009**	YES	**< 0.3**	**< 2**
[1] JSSC 2006	0.8 – 6	<3.5	18 – 20	?	>-3.5	12.5	90nm 2.5V	2 ?	YES	> 6 [3]	?
[2] CICC 2005	0.9 – 5	< 3.5	18 – 19	+4 (sim)	+1 (sim)	12	0.18µm 1.8V	4 ~0.4	YES	?	?
[3] RFIC 2005	2.7 – 4.5	< 5	18 – 19.6	?	-8	16.2 (12.6)	90nm 1.2V	1 0.2	YES	?	?
[5] MTT-S 2005	0.8 – 2.5	< 4 [1]	S_{ds21} ≈ -4	high	high	passive balun	0.18µm -	2 0.073	YES	< 0.4	< 3.2
[6] MTT-S 2005	1.5 – 3.5	< 1 [1]	S_{ds21} ≈ -1	high	high	passive balun	GaAs -	6 0.42	YES	< 1.3	< 4
[4] JSSC 2004	0.2 – 2.0	< 2.4	10 – 14	+12	0	35	0.25µm 2.5V	– 0.075	NO	N/A	N/A
[7] ISSCC 2006	0.5 – 8.2	< 2.6	22 – 25	?	-4 / -16	42	90nm 2.7V	– 0.025	NO	N/A	N/A

[1] Insertion Loss [2] CMOS unless specified differently [3] As derived from component values in schematic

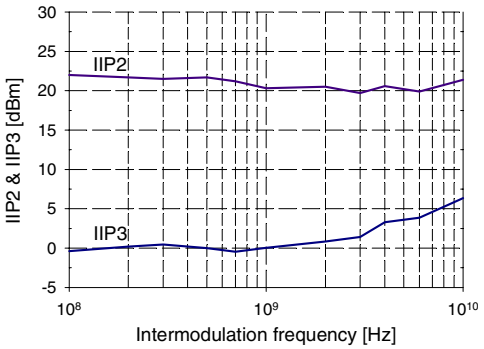

Figure 8. IIP2 and IIP3 versus intermodulation frequency.

The high IIP2 of more than +20dBm over the full 100M–10GHz range can be explained as follows. The non-linear currents which the CG-transistor produces are canceled in exactly the same way as its noise is canceled. This is obvious if one observes that both effects (non-linearity and noise) can be modeled as a voltage controlled current source between source and drain of the CG-transistor. The remaining source of 2nd order non-linearity is the CS-transistor. Transistors in deep submicron processes are known for their low and non-linear output impedance. Thanks to this, a CS-stage with a resistive load reaches a maximum in gain at a certain V_{GS}. Around this maximum the derivative of the gain to V_{GS} is close to zero. Consequently, 2nd order distortion will become small, as it is directly proportional to this derivative. The high IIP2 is obtained by biasing the CS-stage close to the maximum gain point. The spread of IIP2 was measured on 20 samples, while keeping the biasing fixed. The worst-case was found to be +18dBm while other samples showed an IIP2 as high as +34dBm.

VII. CONCLUSIONS

Table I shows a comparison of the balun-LNA to three other wideband CMOS active baluns [1-3], two passive baluns implemented in CMOS [5] and GaAs [6] and two wideband inductorless single-ended LNAs [4,7]. The proposed balun-LNA is more wideband than the passive integrated baluns [5,6] while showing smaller gain and phase imbalances. The LNA performance of the implemented circuit is competitive to non-balun LNAs [4] and [7]. The circuit is integrated in a digital baseline 65nm process using a 1.2V supply voltage. Still, at this low supply voltage, it achieves high linearity and the active area is small, as no integrated inductors are required. In contrast to [1] the balun-LNA presented in this work simultaneously achieves impedance matching, noise canceling and a well balanced output.

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