Design Problem 2

Due Date: In class, Friday, July 25, 2003

Description:

You are to select one of the references on integrated circuit frequency synthesizers from the attached list. You should carefully read the reference and write a report on this paper as described below.

Tasks:

1.) Inform your instructor via e-mail of your choice of reference by suggesting several numbers in order of preference from the list at the end of this assignment. Your instructor will then approve your reference and you may continue this problem.

2.) Carefully read the reference.

3.) Write a short report (no more than five pages including figures) that addresses the following questions?

a.) What is the type of frequency synthesizer architecture used?

b.) What is/are the unique feature/features of this frequency synthesizer (i.e. what makes it different from other frequency synthesizers? Why was the paper published?)

c.) Describe the blocks used in the frequency synthesizer.

d.) Are any external components required to make the synthesizer work? If so what are they?

e.) Summarize the experimental performance in the following table. (This table will be incorporated into a master table by your instructor so please do not adjust the column widths.) You will have to figure out how to convert the data in the paper to the table requirements. If this is not possible, explain why not and provide alternate data.

Ref. No.†	V_{DD} (V)	Tech-nology* (min. L)	Output Freq. Range (GHz)	Ref. Freq. (MHz)	Phase Noise (dBc/Hz) @ 1MHz	Spurious Tones (dBc/Hz)	Settling Time (nsec.)	Power (mW)	Die Area (X mm x Y mm)**

† This is the reference number of the paper assigned to you by your instructor.
* If not CMOS then also include the technology, i.e. BiCMOS, BJT, or GaAs
** Give the area as the sides of a square, for example 1.4mm x 2mm.

Grading

The report will be graded as follows with equal weighting to each category:

1.) Suitability of the paper you picked. Does it represent the general subject of frequency synthesizers? Is the paper trivial or complex?

2.) The use of concepts learned in ECE 6440 to understand and interpret the paper. Did you use any of the concepts and tools learned in the class in writing your report?

3.) The general understanding of the paper. Do you truly know how the frequency synthesizer works and do you understand the unique features and their significance? (The answers to these questions are always found in the ability to clearly and succinctly explain the material to others not familiar with it.)

4.) The quality and organization of the report. The report should follow the general guidelines of an engineering report. This category includes timeliness. You are encouraged to submit your report electronically.

List of Papers on Frequency Synthesizers from IEEE Journal of Solid-State Circuits from 1998 to 2003

1.) C.-H. Heng and B.-S. Song, A 1.8 GHz CMOS Fractional-*N* Frequency Synthesizer with Randomized Multiphase VCO, IEEE Journal of Solid-State Circuits, vol. 38, pp. 848-854, June 2003

2.) B. Zhang, P.E. Allen, and J.M. Huard, A Fast Switching PLL Frequency Synthesizer with an On-Chip Passive Discrete-Time Loop Filter in 0.25μm CMOS, IEEE Journal of Solid-State Circuits, vol. 38, pp. 855-864, June 2003.

3.) K. Shu, E. Sanchez-Sinencio, J. Silva-Martinez, and S.H.K. Embabi, A 2.4 GHz Monolithic Fractional-*N* Frequency Syunthesizer with Robust Phase-Switching Prescaler and Loop Capacitance Multiplier, IEEE Journal of Solid-State Circuits, vol. 38, pp. 866-874, June 2003.

4.) A. Torosyan, D. Fu, and A.N. Willson, Jr., A 300-MHz Quadrature Direct Digital Synthesizer/Mixer in 0.25μm CMOS, IEEE Journal of Solid-State Circuits, vol. 38, pp. 875-887, June 2003.

5.) T.C. Lee and B. Razavi, Astabilization Technique for Phase-Locked Frequency Synthesizers, IEEE Journal of Solid-State Circuits, vol. 38, pp. 888-894, June 2003.

6.) E. Hegazi and A.A. Abidi, A 17-mW Transmitter and Frequency Synthesizer for 900-MHz GSM Fully Integrated in 0.35-μm CMOS, IEEE Journal of Solid-State Circuits, vol. 38, pp. 782, 792, May 2003.

7.) R. Ahola and K. Halonen, A 1.76-GHz 22.6-mW ΔΣ Fractional-N Frequency Synthesizer, IEEE Journal of Solid-State Circuits, vol. 38, pp. 138-140, January 2003.

8.) Paul van Zeijl, Jan-Wim Th. Eikenbroek, Peter-Paul Vervoort, Suma Setty, Jurjen Tangenberg, Gary Shipton, Eric Kooistra, Ids C. Keekstra, Didier Belot, Klaas Visser, Erwin Bosma, Stephan C. Blaakmeer; A Bluetooth radio in 0.18-μm CMOS, IEEE Journal of Solid-State Circuits, vol. 37, pp. 1679 - 1687, December 2002.

9.) Ahmed Nader Mohieldin, Ahmed A. Emira, Edgar Sanchez-Sinencio; A 100-MHz 8-mW ROM-less quadrature direct digital frequency synthesizer, IEEE Journal of Solid-State Circuits, vol. 37, pp. 1235 - 1243, October 2002.

10.) Terng-Yin Hsu, Terng-Ren Hsu, Chung-Cheng Wang, Yi-Chuan Liu, Chen-Yi Lee; Design of a wide-band frequency synthesizer based on TDC and DVC techniques, IEEE Journal of Solid-State Circuits, vol. 37, pp. 1244 - 1255, October 2002.

11.) Jiandong Jiang, Edward K. F. Lee; A low-power segmented nonlinear DAC-based direct digital frequency synthesizer, IEEE Journal of Solid-State Circuits, vol. 37, pp. 1326 - 1330, October 2002.

12.) Augusto Gutierrez-Aitken, Jim Matsui, Eric N. Kaneshiro, Bert K. Oyama, Donald Sawdai, Aaron K. Oki, Dwight C. Streit; Ultrahigh-speed direct digital synthesizer using InP DHBT technology, IEEE Journal of Solid-State Circuits, vol. 37, pp. 1115 - 1119,

September 2002.

13.) Toby K. K. Kan, Gerry C. T. Leung, Howard C. Luong; A 2-V 1.8-GHz fully integrated CMOS dual-loop frequency synthesizer, IEEE Journal of Solid-State Circuits, vol. 37, pp. 1012 - 1020, August 2002.

14.) Michael H. Perrott, Mitchell D. Trott, Charles G. Sodini; A modeling approach for Σ--Δ fractional-N frequency synthesizers allowing straightforward noise analysis, IEEE Journal of Solid-State Circuits, vol. 37, pp. 1028 - 1038, August 2002.

15.) Dorin Emil Calbaza, Yvon Savaria; A direct digital period synthesis circuit, IEEE Journal of Solid-State Circuits, vol. 37, pp. 1039 - 1045, August 2002.

16.) Bram De Muer, Michel S. J. Steyaert; A CMOS monolithic ΔΣ-controlled fractional-N frequency synthesizer for DCS-1800, IEEE Journal of Solid-State Circuits, vol. 37, pp. 835 - 844, July 2002.

17.) Nicola Da Dalt, Sven Derksen, Patrizia Greco, Christoph Sandner, Harald Schmid, Klaus Strohmayer; A fully integrated 2.4-GHz LC-VCO frequency synthesizer with 3-ps jitter in 0.18-?m standard digital CMOS copper technology, IEEE Journal of Solid-State Circuits, vol. 37, pp. 959 - 962, July 2002.

18.) Yido Koo, Hyungki Huh, Yongsik Cho, Jeongwoo Lee, Joonbae Park, Kyeongho Lee, Deog-Kyoon Jeong, Wonchan Kim; A fully integrated CMOS frequency synthesizer with charge-averaging charge pump and dual-path loop filter for PCS- and cellular-CDMA wireless systems, IEEE Journal of Solid-State Circuits, vol. 37, pp. 536 - 542, May 2002.

19.) Chi-Wa Lo, Howard Cam Luong; A 1.5-V 900-MHz monolithic CMOS fast-switching frequency synthesizer for wireless applications, IEEE Journal of Solid-State Circuits, vol. 37, pp. 459 - 470, April 2002.

20.) Woogeun Rhee, Biagio Bisanti, Akbar Ali; An 18-mW 2.5-GHz/900-MHz BiCMOS dual frequency synthesizer with <10-Hz RF carrier resolution, IEEE Journal of Solid-State Circuits, vol. 37, pp. 515 - 520, April 2002.

21.) Bernd-Ulrich H. Klepser, Markus Scholz, Edmund Götz; A 10-GHz SiGe BiCMOS phase-locked-loop frequency synthesizer, IEEE Journal of Solid-State Circuits, vol. 37, pp. 328 - 335, March 2002.

22.) Anne Spataro, Yann Deval, Jean-Baptiste Bégueret, Pascal Fouillat, Didier Belot; A VLSI CMOS delay oriented waveform converter for polyphase frequency synthesizer, IEEE Journal of Solid-State Circuits, vol. 37, pp. 336 - 341, March 2002.

23.) Daniel R. McMahill, Charles G. Sodini; A 2.5-Mb/s GFSK 5.0-Mb/s 4-FSK Automatically calibrated Σ--Δ frequency synthesizer, IEEE Journal of Solid-State Circuits, vol. 37, pp. 18 - 26, January 2002.

24.) Jeffrey A. Weldon, R. Sekhar Narayanaswami, Jacques C. Rudell, Li Lin, Masanori Otsuka, Sebastien Dedieu, Luns Tee, King-Chun Tsai, Cheol-Woong Lee, Paul R. Gray; A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers, IEEE Journal of Solid-State Circuits, vol. 36, pp. 2003 - 2015, December 2001.

25.) Hooman Darabi, Shahla Khorram, Hung-Ming Chien, Meng-An Pan, Stephen Wu, Shervin Moloudi, John C. Leete, Jacob J. Rael, Masood Syed, Robert Lee, Brima Ibrahim, Maryam Rofougaran, Ahmadreza Rofougaran; A 2.4-GHz CMOS transceiver for Bluetooth, IEEE Journal of Solid-State Circuits, vol. 36, pp. 2016 - 2024, December 2001.

26.) Adrian Maxim, Baker Scott, Edmund M. Schneider, Melvin L. Hagge, Steven Chacko, Dan Stiurca; A low-jitter 125--1250-MHz process-independent and ripple-poleless 0.18-µm CMOS PLL based on a sample--Reset loop filter, IEEE Journal of Solid-State Circuits, vol. 36, pp. 1673 - 1683, November 2001.

27.) Wolfgang Thomann, Josef Fenk, Richard Hagelauer, Robert Weigel; Fully integrated W-CDMA IF receiver and IF transmitter including IF synthesizer and on-chip VCO for UMTS mobiles, IEEE Journal of Solid-State Circuits, vol. 36, pp. 1407 - 1419, September 2001.

28.) Walter T. Bax, Miles A. Copeland; A GMSK modulator using a ΔΣ frequency discriminator-based synthesizer, IEEE Journal of Solid-State Circuits, vol. 36, pp. 1218 - 1227, August 2001.

29.) Hideyuki Nosaka, Yo Yamaguchi, Akihiro Yamagishi, Hiroyuki Fukuyama, Masahiro Muraguchi; A low-power direct digital synthesizer using a self-adjusting phase-interpolation technique, IEEE Journal of Solid-State Circuits, vol. 36, pp. 1281 - 1285, August 2001.

30.) Lizhong Sun, Tadeusz A. Kwasniewski; A 1.25-GHz 0.35-?m monolithic CMOS PLL based on a multiphase ring oscillator, IEEE Journal of Solid-State Circuits, vol. 36, pp. 910 - 916, June 2001.

31.) Chan-Hong Park, Ook Kim, Beomsup Kim; A 1.8-GHz self-calibrated phase-locked loop with precise I/Q matching, IEEE Journal of Solid-State Circuits, vol. 36, pp. 777 - 783, May 2001.

32.) David J. Foley, Michael P. Flynn; CMOS DLL-Based 2-V 3.2-ps jitter 1-GHz clock synthesizer and temperature-compensated tunable oscillator, IEEE Journal of Solid-State Circuits, vol. 36, pp. 417 - 423, March 2001.

33.) Tsung-Hsien Lin, William J. Kaiser; A 900-MHz 2.5-mA CMOS frequency synthesizer with an automatic SC tuning loop, IEEE Journal of Solid-State Circuits, vol. 36, pp. 424 - 431, March 2001.

34.) William S. T. Yan, Howard C. Luong; A 2-V 900-MHz monolithic CMOS dual-loop frequency synthesizer for GSM receivers, IEEE Journal of Solid-State Circuits, vol. 36, pp. 204 - 216, February 2001.

35.) George Chien, Paul R. Gray; A 900-MHz local oscillator using a DLL-based frequency multiplier technique for PCS applications, IEEE Journal of Solid-State Circuits, vol. 35, pp. 1996 - 1999, December 2000.

36.) William B. Wilson, Un-Ku Moon, Kadaba R. Lakshmikumar, Liang Dai; A CMOS self-calibrating frequency synthesizer, IEEE Journal of Solid-State Circuits, vol. 35, pp. 1437 - 1444, October 2000.

37.) Ching-Yuan Yang, Shen-Iuan Liu; Fast-switching frequency synthesizer with a discriminator-aided phase detector, IEEE Journal of Solid-State Circuits, vol. 35, pp. 1445 - 1452, October 2000.

38.) Woogeun Rhee, Bang-Sup Song, Akbar Ali; A 1.1-GHz CMOS fractional-N frequency synthesizer with a 3-b third-order ΔΣ modulator, IEEE Journal of Solid-State Circuits, vol. 35, pp. 1453 - 1460, October 2000.

39.) Guang-Kaai Dehng, Ching-Yuan Yang, June-Ming Hsu, Shen-Iuan Liu; A 900-MHz 1-V CMOS frequency synthesizer, IEEE Journal of Solid-State Circuits, vol. 35, pp. 1211 - 1214, August 2000.

40.) Hugh Mair, Liming Xiu; An architecture of high-performance frequency and phase synthesis, IEEE Journal of Solid-State Circuits, vol. 35, pp. 835 - 846, June 2000.

41.) Hamid R. Rategh, Hirad Samavati, Thomas H. Lee; A CMOS frequency synthesizer with an injection-locked frequency divider for a 5-GHz wireless LAN receiver, IEEE Journal of Solid-State Circuits, vol. 35, pp. 780 - 787, May 2000.

42.) Christopher Lam, Behzad Razavi; A 2.6-GHz/5.2-GHz frequency synthesizer in 0.4-μm CMOS technology, IEEE Journal of Solid-State Circuits, vol. 35, pp. 788 - 794, May 2000.

43.) Cicero S. Vaucher; An adaptive PLL tuning system architecture combining high spectral purity and fast settling time, IEEE Journal of Solid-State Circuits, vol. 35, pp. 490 - 502, April 2000.

44.) Abdellatif Bellaouar, Michael S. O'brecht, Amr M. Fahim, Mohamad I. Elmasry; Low-power direct digital frequency synthesis for wireless communications, IEEE Journal of Solid-State Circuits, vol. 35, pp. 385 - 390, March 2000.

45.) Hee-Tae Ahn, David J. Allstot; A low-jitter 1.9-V CMOS PLL for UltraSPARC microprocessor applications, IEEE Journal of Solid-State Circuits, vol. 35, pp. 450 - 454, March 2000.

46.) Patrik Larsson; A 2-1600-MHz CMOS clock recovery PLL with low-Vdd capability, IEEE Journal of Solid-State Circuits, vol. 34, pp. 1951 - 1960, December 1999.

47.) Siamak Mortezapour, Edward K. F. Lee; Design of low-power ROM-less direct digital frequency synthesizer using nonlinear digital-to-analog converter, IEEE Journal of Solid-State Circuits, vol. 34, pp. 1350 - 1359, October 1999.

48.) Avanindra Madisetti, Alan Y. Kwentus, Alan N. Willson Jr.; A 100-MHz, 16-b, direct digital frequency synthesizer with a 100-dBc spurious-free dynamic range, IEEE Journal of Solid-State Circuits, vol. 34, pp. 1034 - 1043, August 1999.

49.) Terng-Yin Hsu, Bai-Jue Shieh, Chen-Yi Lee; An all-digital phase-locked loop (ADPLL)-based clock recovery circuit, IEEE Journal of Solid-State Circuits, vol. 34, pp. 1063 - 1073, August 1999.

50.) Wei-Zen Chen, Jieh-Tsorng Wu; A 2-V, 1.8-GHz BJT phase-locked loop, IEEE Journal of Solid-State Circuits, vol. 34, pp. 784 - 789, June 1999.

51.) Chan-Hong Park, Beomsup Kim; A low-noise, 900-MHz VCO in 0.6-?m CMOS, IEEE Journal of Solid-State Circuits, vol. 34, pp. 586 - 591, May 1999.

52.) Jan Craninckx, Michel Steyaert; A fully integrated CMOS DCS-1800 frequency synthesizer, IEEE Journal of Solid-State Circuits, vol. 33, pp. 2054 - 2065, December 1998.

53.) Arvin R. Shahani, Derek K. Shaeffer, S. S. Mohan, Hirad Samavati, Himad R. Rategh, Maria del Mar Hershenson, Min Xu, C. Patrick Yue, Daniel J. Eddleman, Mark A. Horowitz, Thomas H. Lee; Low-power dividerless frequency synthesis using aperture phase detection, IEEE Journal of Solid-State Circuits, vol. 33, pp. 2232 - 2239, December 1998.

54.) Chris Diorio, Todd Humes, Johannes K. Notthoff, Gregory Chao, Alex Lai, John D. Hyde, Mark Kintis, Aaron Oki; A low-noise, GaAs/AlGaAs, microwave frequency-synthesizer IC, IEEE Journal of Solid-State Circuits, vol. 33, pp. 1306 - 1312, September 1998.

55.) Cicero Vaucher, Dieter Kasperkovitz; A wide-band tuning system for fully integrated satellite receivers, IEEE Journal of Solid-State Circuits, vol. 33, pp. 987 - 997, July 1998.

56.) Norman M. Filiol, Thomas A. D. Riley, Calvin Plett, Miles A. Copeland; An agile ISM band frequency synthesizer with built-in GMSK data modulation, IEEE Journal of Solid-State Circuits, vol. 33, pp. 998 - 1008, July 1998.

57.) Ahmadreza Rofougaran, Glenn Chang, Jacob J. Rael, James Y.-C. Chang, Maryam Rofougaran, Paul J. Chang, Masoud Djafari, Edward W. Roth, Asad A. Abidi, Henry Samueli; A single-chip 900-MHz spread-spectrum wireless transceiver in 1-μm CMOS--Part I: Architecture and transmitter design, IEEE Journal of Solid-State Circuits, vol. 33, pp. 515 - 534, April 1998.

58.) Francesco Piazza, Qiuting Huang; A 1.57-GHz RF front-end for triple conversion GPS receiver, IEEE Journal of Solid-State Circuits, vol. 33, pp. 202 - 209, February 1998.

59.) Akihiro Yamagishi, Masayuki Ishikawa, Tsuneo Tsukahara, Shigeru Date; A 2-V, 2-GHz low-power direct digital frequency synthesizer chip-set for wireless communication, IEEE Journal of Solid-State Circuits, vol. 33, pp. 210 - 217, February 1998.

60.) Jouko Vankka, Mikko Waltari, Marko Kosunen, Kari A. I. Halonen; A direct digital synthesizer with an on-chip D/A-converter, IEEE Journal of Solid-State Circuits, vol. 33, pp. 218 - 227, February 1998.

61.) Janusz Nieznanski; An alternative approach to the ROM-less direct digital synthesis, IEEE Journal of Solid-State Circuits, vol. 33, pp. 169 - 170, January 1998.