EXAMINATION NO. 1

NAME_____SCORE_____/100

INSTRUCTIONS: This exam is lecture notes (the ones handed out). The exam consists of 4 questions for a total of 100 points. Please show your work leading to your answers so that maximum partial credit may be given where appropriate. Be sure to turn in your exam with the problems in numerical order, firmly attached together.

Problem 1 - (25 points)

Short questions. The point worth of the question is given in parentheses.

a.) (7) Explain clearly and concisely the difference between direct frequency synthesis and indirect frequency synthesis.

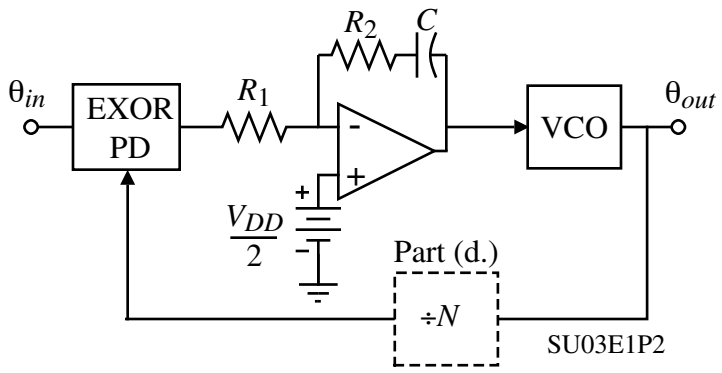
b.) (7) Why are direct synthesizers able to change frequencies much faster than indirect synthesizers? Explain.

c.) (6) Compare the characteristics, disadvantages and advantages of the linear multiplier phase detector, the EXOR phase detector, the JK phase detector, and the phase frequency detector.

d.) (5) Compare the disadvantages and advantages of a charge pump and a filter in a PLL application.

Problem 2 - (25 points)

Consider the PLL shown. Assume that: 1.) the phase detector is a simple CMOS EXOR whose logic levels are ground and V_{DD} = 5V, 2.) both the input to the loop and the VCO output are square waves that swing between ground andV_{DD}, and 3.) that the VCO has a perfectly linear relationship between the control voltage and output frequency of 10 MHz/V. The polarities are such that an increase in control voltage causes an increase in the VCO frequency.



(a.) Derive the expression for the open-loop transmission and the transfer function $\theta_{out}(s)/\theta_{in}(s)$.

(b.) Initially assume $R_2 = 0$ and $R_1 = 10\text{k}\Omega$. What value of C gives a loop crossover frequency of 100kHz? What is the phase margin. Assume the op amp is ideal.

(c.) With the value of C from part (b.), what value of R_2 will provide a phase margin of 45° while preserving a 100 kHz crossover frequency.

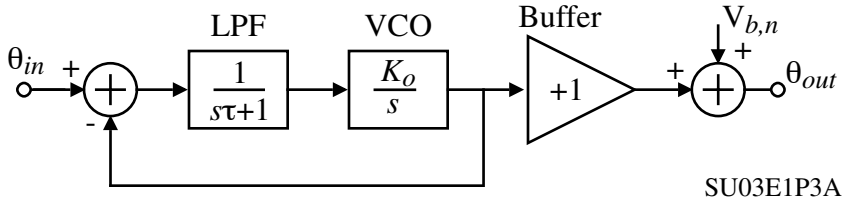
(d.) Now assume that a frequency divider of factor N is inserted into the feedback path. With the component values of part (c.), what is the largest value of N that can be tolerated without shrinking the phase margin below 14°?

Problem 3 - (25 points)

In many practical applications, it is necessary to buffer the VCO output signal. Assume that the buffer has a voltage gain of 1 and its output is corrupted by an additive white noise noise voltage of $V_{b,n}$.

(a.) Find the output phase, $\theta_{out}(s)$, as a function of the input phase $\theta_{in}(s)$ and the output noise of the buffer, $V_{b,n}$, for the PLL shown with the buffer outside of the PLL loop.

Give an approximate sketch for magnitude response of $\theta_{out}(j\omega)/V_{b,n}$ assuming $\zeta = 0.707$.



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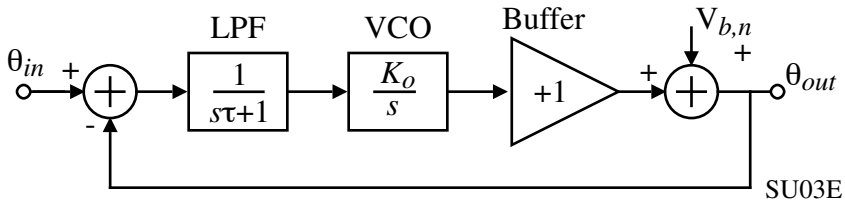
(b.) Find the output phase, $\theta_{out}(s)$, as a function of the input phase $\theta_{in}(s)$ and the output noise of the buffer, $V_{b,n}$, for the PLL shown with the buffer outside of the PLL loop.

Give an approximate sketch for magnitude response of $\theta_{out}(j\omega)/V_{b,n}$ assuming $\zeta = 0.707$.



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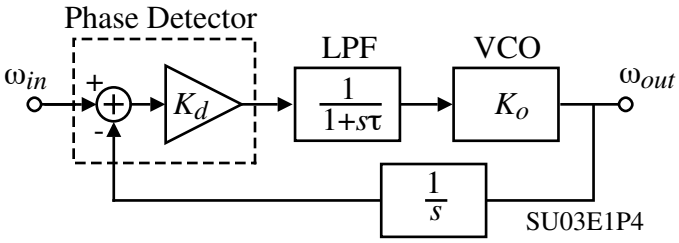
(c.) Which of the two PLL architectures leads to an output spectrum with less noise assuming that the input and VCO are noise free? How would your answer change if the input signal to the PLL was noisy? Why?

Problem 4 - (25 points)

A linear model of a PLL is shown. (a.) Solve for the closed-loop transfer function of $\omega_{out}(s)/\omega_{in}(s)$. Compare this transfer function with the following general transfer function and identify , H, ω_n, and ζ.



$$\frac{\omega_{out}(s)}{\omega_{in}(s)} = \frac{H\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

(b.) If $\zeta < 1$, the step response to $\omega_{in}(t) = \Delta\omega \cdot \mu(t)$ is given as

$$\omega_{out}(t) = H\left[1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin\left(\omega_n\sqrt{1-\zeta^2}\,t + \theta\right)\right] \text{ where } \theta = \sin^{-1}\sqrt{1-\zeta^2}$$

Assume that $K_v = K_o K_d = 63.58\text{x}10^3$ rads/sec. and $\tau = 8\mu$sec. If the output frequency is to be changed from 901 MHz to 901.2 MHz, how long does the PLL output frequency take to settle with 100 Hz of its final value? Simplify your analysis by assuming worst case conditions (i.e. Maximum value of $\sin(x) = 1$).

Extra Sheet