Homework Assignment No. 2 - Solution

Problem 1 - (10 points)

A phase-locked loop has a center frequency of 10^5 rads/s, a K_o of 10^3 rad/V-s, and a K_d of 1 V/rad. Assume there is no other gain in the loop. Determine the loop bandwidth in the first-order loop configuration. Determine the single-pole, loop-filter pole location to give the closed-loop poles located on 45° radials from the origin of the complex frequency plane.

Solution

The loop bandwidth = $K_v = K_o K_p = \dfrac{10^3}{\text{s}}$

In order to produce poles at 45° to the axis, we add a loop filter pole at ω_1 where

$$\omega_1 = 2K_v = 2000 \text{ rads/sec.}$$

The filter transfer function becomes,

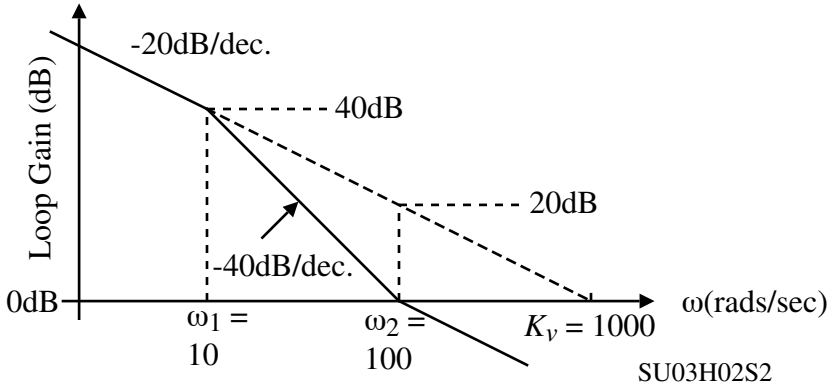
$$F(s) = \frac{\omega_1}{s+\omega_1} = \frac{2000}{s+2000}$$

Problem 2 – (10 points)

For the same PLL of the previous problem, design a loop filter with a zero that gives a crossover frequency for the loop gain of 100 rads/sec. The loop phase shift at the loop crossover frequency should be –135°.

Solution

A plot of the desired loop gain is shown below.



SU03H02S2

If ω_2 (the zero frequency) is at the unity gain point, then the loop phase shift will be –135° at this point. Therefore, we require that $\omega_2 = 100$ radians/sec.. If $\omega_1 = 10$ radians/sec., the requirement will be satisfied as shown in the above plot.

The design of the filter becomes,

$$\omega_2 = \frac{1}{R_2 C} \quad \text{and} \quad \omega_1 = \frac{1}{(R_1+R_2)C}$$

$$\therefore \quad \frac{\omega_2}{\omega_1} = 1 + \frac{R_1}{R_2} = 10 \quad \rightarrow \quad R_1 = 9R_2$$

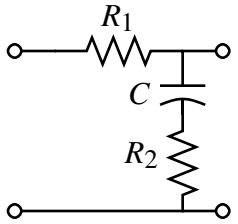


Fig. SU03H02S2A

Now appropriate values of R_1 , R_2, and C can be chosen.

Problem 3 – (10 points)

Estimate the capture range of the PLL of the previous problem assuming that it is not artificially limited by the VCO frequency range.

Solution

For capture we need

$$|(\omega_i - \omega_o)| < \frac{\pi}{2} Kv|F(j(\omega_i - \omega_o)|$$

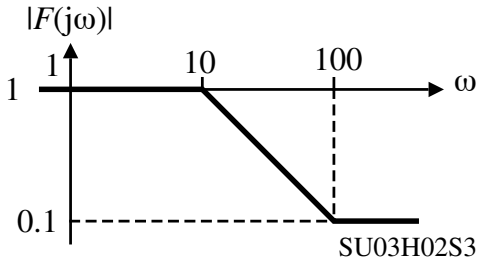
If we assume that

$$|(\omega_i - \omega_o)| = \frac{\pi}{2} Kv|F(j(\omega_i - \omega_o)|$$

then with $\omega_o = 10^5$ rads/sec and $K_v = 1000$ rads/sec. we get,

$$|(\omega_i - \omega_o)| = 1570|F(j(\omega_i - \omega_o)|$$

Now from the previous problem, we know that $|F(j\omega)|$ is given as



From this figure we can solve the above equation to find that

$(\omega_i - \omega_o) =$ 157 rads/sec.

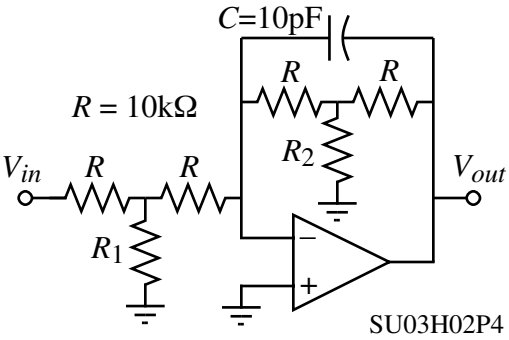
which is the capture range.

Problem 4 – (10 points)

A filter for a phase locked loop is specified as

$$|F(s)| = \frac{10\omega_1}{s+\omega_1} = \frac{1{,}000{,}000}{s+100{,}000}$$

and must be implemented on a CMOS chip using resistors no larger than 10kΩ and capacitors no larger than 10pF. Using the circuit shown, find the values of R_1 and R_2 that will satisfy the component value constraints.



Solution

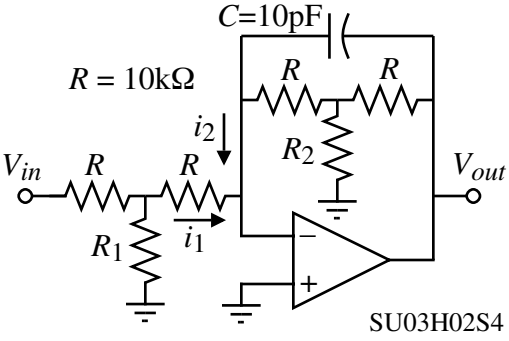
Find the currents i_1 and i_2,

$$i_1 = \frac{v_{in}}{R + \frac{RR_1}{R+R_1}} \frac{R}{R+R_1} = \frac{R_1\, v_{in}}{2RR_1 + R^2} = \frac{v_{in}}{R_{T1}}$$

and

$$i_2 = \frac{v_{out}}{R + \frac{RR_1}{R+R_1}} \frac{R}{R+R_1} + sCv_{out}$$

$$= \frac{R_2\, v_{out}}{2RR_2 + R^2} + sCv_{out} = \frac{v_{out}}{R_{T2}} + sCv_{out}$$



Solving for the sum of the currents flow toward the minus op amp input terminal gives,

$$\frac{v_{in}}{R_{T1}} + \frac{v_{out}}{R_{T2}} + sCv_{out} = 0 \qquad \rightarrow \qquad \frac{v_{out}}{v_{in}} = -\frac{R_{T2}}{R_{T1}} \frac{1}{sCR_{T2}+1} = -10\, \frac{1}{\frac{s}{10^5}+1}$$

$$\therefore \qquad CR_{T2} = 10^{-5} \quad \rightarrow R_{T2} = \frac{10^{-5}}{10^{-11}} = 10^6$$

$$R_{T2} = \frac{2RR_2 + R^2}{R_2} = 2R + \frac{R^2}{R_2} = 20\text{x}10^3 + \frac{100\text{x}10^6}{R_2} = 10^6$$

$$\therefore \qquad R_2 = \frac{100\text{x}10^6}{10^6\text{-}20\text{x}10^3} = \underline{\underline{100\Omega}}$$

$$R_{T1} = \frac{R_{T2}}{10} = 10^5 \qquad \rightarrow \qquad 2R + \frac{R^2}{R_1} = 20\text{x}10^3 + \frac{100\text{x}10^6}{R_1} = 10^5$$

$$\therefore \qquad R_1 = \frac{100\text{x}10^6}{10^5\text{-}20\text{x}10^3} = \underline{\underline{1000\Omega}}$$

This problem shows how a clever circuit technique can make a filter suitable for integrated circuit implementation.

Problem 5 – (20 points)

This homework is designed to provide practical inductor design experience for students. Use ASITIC for the design and analysis. However, other tools are acceptable if they give all the results including layout. (See lecture 045 on Monolithic Inductor Design in Silicon Technology)

A 5GHz LC tank will be designed as a part of LC oscillator. C value is given as 1pF.

(a) Find L value. (b) Design and simulate a spiral inductor with this L value (± 5% range). Optimize design parameters, W, S, D and N to get a high Q (Q_{min} = 5). Show L, Q, f_{SR} value obtained from simulation. (c) Show the layout. (d) Give a lumped circuit model with component values.

Solution

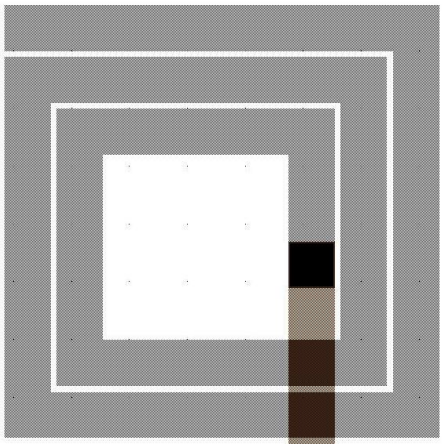
(a) LC tank oscillation frequency is given as 5GHz.

$$L = \frac{1}{\omega_{osc}^2 \cdot C} = \frac{1}{(2\pi \cdot 5\text{x}10^9)(1\text{x}10^{-12})} = 1.01\text{x}10^{-9}$$

(b) One possible solution is

- Parameters: W = 16um, S = 2um, D = 150um, N =2.5
- Resulting inductor: L = 0.952nH, Q = 8.54, f_{SR} = 19.35GHz @ 5GHz

(c) Layout



(d) Pi model from ASITIC is shown below. This is the analysis result from 'pix' command.