Homework No. 8 – Solution

Problem 1 – (50 points)

Use the National Semiconductor website (www.national.com) to design a DPLL frequency synthesizer for the GSM (935-960MHz) application. The channel spacing is 200kHz. Choose an appropriate VCO from a manufacturer. Assume a 0.25μm CMOS process with a 3.3V power supply.

Your homework should show a block diagram for the resulting frequency synthesizer with the blocks identified. Give the following parameters that you selected for your design:

1.) N, the divider ratio.
2.) ζ, the damping ratio
3.) The type of PD/PFD and the value of K_d.
4.) The type of VCO, K_o, and V_{min} and V_{max}.
5.) τ_L, the lock-in time or settling time and ω_n, the natural frequency of the PLL
6.) Design of the loop filter including the time constants and component values.

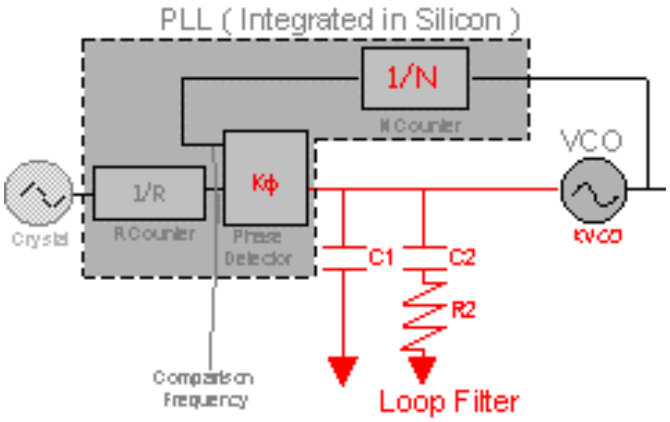
Solution

The problem specifications call for the following:

- Standard : GSM
- Frequency band : 935 MHz ~ 960 MHz
- Channel spacing : 200 kHz
- Power supply : 3.3 V
- Technology : 0.25 μm CMOS
- Switching time : < 800 μs (by GSM standard)

DESIGN

The block diagram for this design is as follows:



The central frequency to use is the geometric mean of the extreme frequencies (947 MHz).

The devices chosen for this design are:

1. A low phase noise PLL (PFD), (chip code LMX2346) from National Semiconductors. This has a range of operation from 200 MHz to 2 GHz, so it is suitable here.
2. A VCO (chip code VCO191-947U) from Vari-L. Its frequency of operation is well-suited for this GSM application: 934 MHz to 960 MHz.

3. A second-order loop filter. This will reduce the number of capacitors in contrast with a higher order filter. And this can be done because the filter components are going to be off-chip, so the needed capacitance values –relatively high– are realizable. This filter is passive so as to avoid the non-idealities associated with an OPAMP (mainly, noise).

The comparison frequency at the input of the phase/frequency detector was chosen to be equal to the channel spacing, i.e., 200 kHz. Therefore, the reference divider —if using a 10 MHz crystal source at the input— and the feedback divider ratio can be found as:

$$R = \frac{f_{CRYSTAL}}{f_{COMPARISON}} = \frac{10\,MHz}{200\,kHz} = 50$$

$$N = \frac{f_{OUTPUT}}{f_{COMPARISON}} = \frac{947\,MHz}{200\,kHz} = 4735$$

Other parameters for this design are:

VCO
- K_0 = 18 MHz/V
- V_{min} = typ. 0.8 V @ 934 MHz (min. 0.4 V)
- V_{max} = typ. 2.2 V @ 960 MHz (min. 2.6 V)

PFD
- K_ϕ (= K_d) = 4 mA (or $4/2\pi$ [mA/rad])

General
- Lock-in time = τ_L = 200 μs

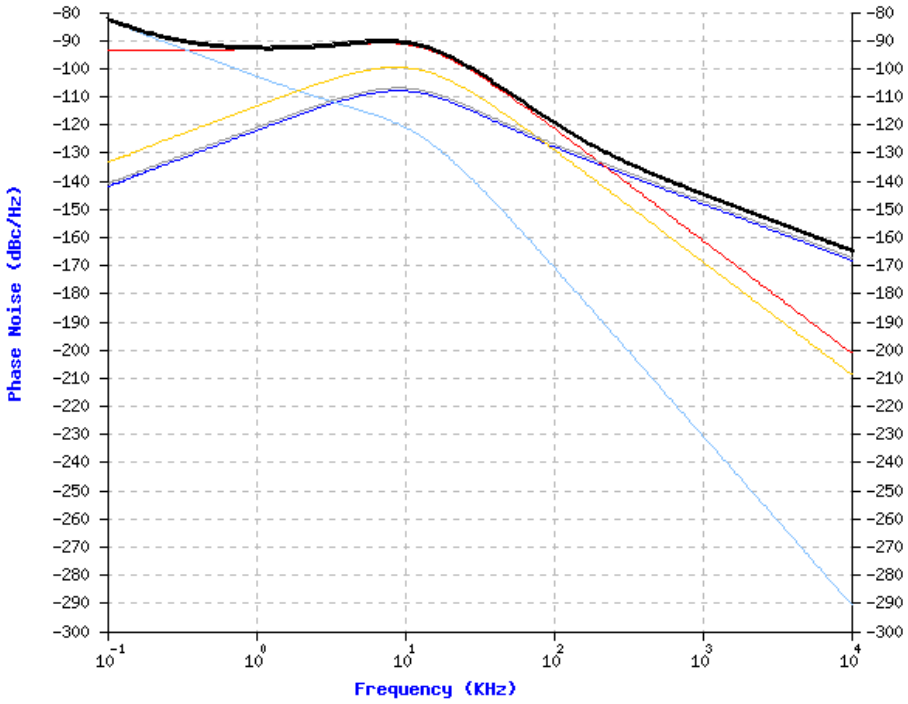
The filter components were found to be (standard values given, ideal values in parenthesis):

C_1 = 910 pF (943.6 pF)
C_2 = 6.8 nF (6.6 nF)
R_2 = 5.6 kΩ (5.7 kΩ)

SIMULATION RESULTS

Simulation was performed using the computed *standard* values for the filter components and are as follows:

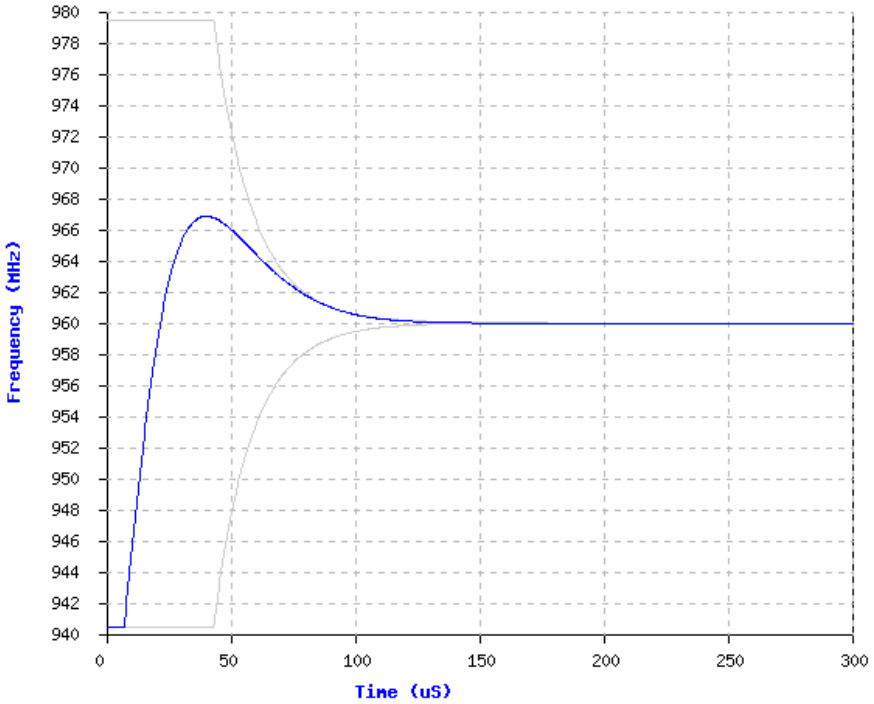
Phase Noise performance:
- 0 dB bandwidth = 14.80 kHz
- Peak frequency = 7.40 kHz
- Phase noise peaking = 2.47 dB
- Phase noise @ 10 kHz offset = -90.56 dB_c/Hz
- Phase noise @ 100 kHz offset = -118.86 dB_c/Hz
- RMS phase error = 0.33°



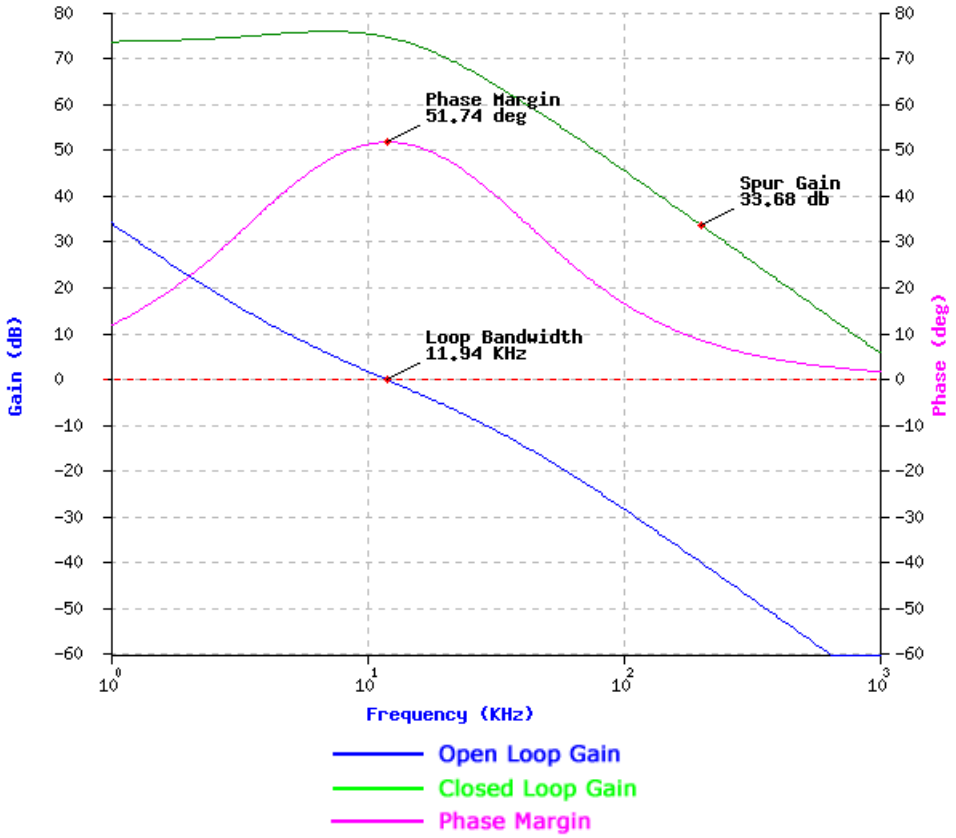
— Total noise — PLL noise
— VCO noise — TCXO noise
— R_2 noise

Lock-in time performance for a frequency jump from 934 MHz to 960 MHz (worst case) with a tolerance of 500 Hz:

- Lock-in time = τ_L = 215.31 μs



Frequency analysis (Bode plots):



- Natural frequency = ω_n = 7.06 kHz
- Phase margin = 51.74°
- Spur gain at comparison frequency = 33.68 dB
- Loop bandwidth = 11.94 kHz
- Damping factor = ζ = 0.84

Spur level estimation

Spur Offset (kHz)	Description	Spur Gain (dB)	Leakage Component (dB_c)	Pulse Component (dB_c)	Spur Level (dB_c)
200	1st Spur	33.7	-90.5	-76.3	-76.1
400	2nd Spur	21.7	-102.4	-81.2	-81.1
600	3rd Spur	14.7	-109.4	-84.2	-84.2

Therefore, this design is suitable for use in the proposed GSM application.

Problem 2 – (10 points)

The phase noise of an oscillator is –40 dBc at 10 Hz offset and has a straight-line variation (on a dBc vs. log$f$ scale) variation to –85 dBc at 15 kHz offset. Determine the residual phase modulation in the range of 300 Hz to 3 kHz.

Solution

We will solve this problem modeling the phase noise as a simple line on the dBc vs. log f scale as $y = mx + b$ where

y = dBc and $x = \log f$

The slope of the curve on the dBc vs. log f scale is found as,

$$m = \frac{-85 - (-40)}{\log(15\text{x}10^3) - \log(10)} = -14.186 \text{ dB/dec.}$$

The intercept, b, can be found as

$$-40 = (-14.186 \text{ dB/dec.})\log(10) + b$$

$$b = -40 + (14.186 \text{ dB/dec})\log(10) = -40 + 14.186 = -25.832 \text{ dBc}$$

$\therefore$ y(dBc) = -14.186 dBc/dec (log$f$) – 25.832 dBc

Let $y = \mathcal{L}\{f\}$ dBc

We can write for both sidebands $\mathcal{L}\{f\} = 2(10^{-(25.832/10)})\, f^{-1.4186}$

Integrating from 300Hz to 3kHz, gives the residual PM,

$$\theta_{rms} = \sqrt{\int_{300}^{3000} 2[10^{-(25.832/10)}]\, f^{-1.4186}\, df} = 0.027 \text{ radians}$$

Problem 3 – (10 points)

On page 160-33 of the class lecture notes, the approximate *rms* value of the impulse sensitivity function for single-ended ring oscillators is given as

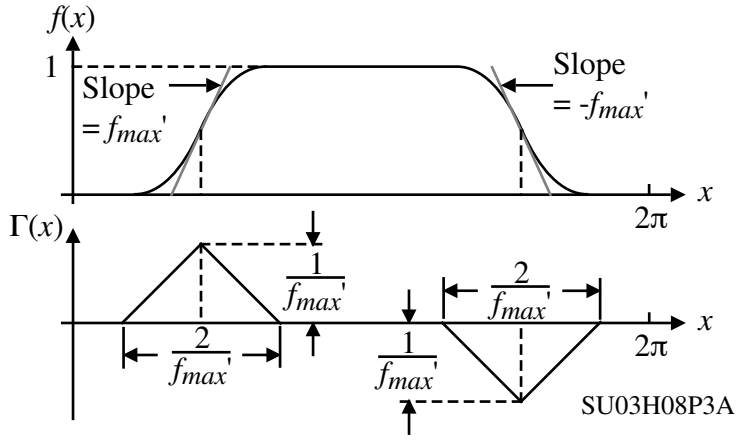
$$\Gamma_{rms} \approx \sqrt{\frac{2\pi^2}{3\eta^3}}\, \frac{1}{N^{1.5}}$$

Derive this approximate impulse sensitivity function.

Solution

This derivation follows that given in A. Hajimiri, et. al., "Jitter and Phase Noise in Ring Oscillators," *IEEE J. of Solid-State Circuits*, vol. 34, no. 6, June 1999, pp. 790-804.

The approximate waveform and the ISF for a single-ended ring oscillator is shown below and is based on the assumptions that the sensitivity during the transition is inversely proportional to the slope and the rise and fall times are symmetrical.



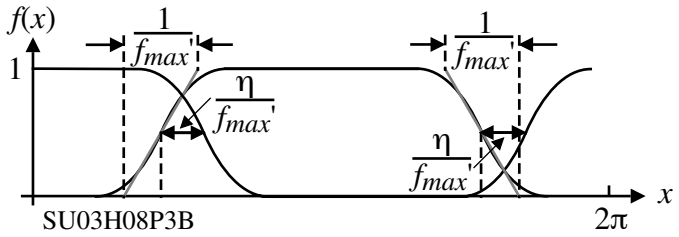
The Γ_{rms} can be estimated as,

$$\Gamma_{rms}^2 \approx \frac{1}{2\pi}\int_0^{2\pi}\Gamma^2(x)dx = \frac{1}{4\pi}\int_0^{1/f_{max}'}x^2dx = \frac{2}{3\pi}\left(\frac{1}{f_{max}'}\right)^3$$

The normalized delay per stage is given as

$$\hat{t}_D = \frac{\eta}{f_{max}'}$$

which is found from the following waveforms of the single-ended ring oscillator.



The period of the ring oscillator is $2N$ times larger than the normalized delay per stage and is

$$2\pi = 2N\hat{t}_D = \frac{2N\eta}{f_{max}'} \qquad \rightarrow \qquad \frac{1}{f_{max}'} = \frac{\pi}{N\eta}$$

$$\therefore \qquad \Gamma_{rms}^2 \approx \frac{2}{3\pi}\left(\frac{\pi}{N\eta}\right)^3 = \frac{2\pi^2}{3\eta^3}\frac{1}{N^3}$$

The result is obtained as,

$$\boxed{\Gamma_{rms} \approx \sqrt{\frac{2\pi^2}{3\eta^3}}\frac{1}{N^{1.5}}}$$