

Homework No. 9 - Solutions**Problem 1 – (10 points)**

A frequency synthesizer has a reference frequency of 5kHz and uses a 64/65 dual-modulus prescaler. Determine the values of the A and M counters to give an output frequency of 555.015 MHz.

Solution

$$f_o = Nf_r$$

$$N = \frac{f_o}{f_r} = 111003$$

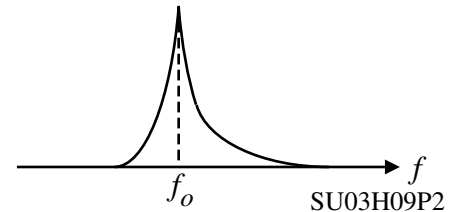
$$N = MP + A$$

$$M = \text{Integer} \left[\frac{N}{P} \right] = \text{Integer} \left[\frac{111003}{64} \right] = 1734, \quad A = N - MP = 27$$

$$\therefore \boxed{A = 27 \text{ and } M = 1734}$$

Problem 2 – (10 points)

When testing a frequency synthesizer, you observe the frequency display shown above on a spectrum analyzer. What important fact is obvious from the display?

Solution

Asymmetrical sidebands indicate the presence of both PM/FM and AM spurs.

Problem 3 – (10 points)

What is the main advantage of a fractional- N PLL synthesizer over an ordinary PLL synthesizer? Explain.

Solution

A fractional- N PLL synthesizer gives much high frequency resolution than possible with an ordinary PLL synthesizer having the same reference frequency.

Problem 4 – (10 points)

A 1600 MHz carrier together with a set of 20 kHz PM spurs are applied to a divide by 8 frequency divider. The power of the 200 MHz carrier frequency output of the divider is 0.2 mW and the 20 kHz spurs have an amplitude of 20 μ V. What is the phase deviation of the signal at the input of the divider? All impedances are 50 ohms.

Solution

At the output,

$$V_s = 20 \times 10^{-6} \text{ V} \quad \text{and} \quad P_o = 0.2 \times 10^{-3} \text{ W}$$

$$\therefore P_s = \frac{|V_s|^2}{50} = 8 \times 10^{-12} \text{ W}$$

$$SSB = 10 \log_{10} \left(\frac{P_s}{P_o} \right) = 10 \log_{10} \left(\frac{8 \times 10^{-12}}{0.2 \times 10^{-3}} \right) = -73.979 \text{ dB}$$

At the input,

$$SSB_{input} = SSB_{output} + 20 \log_{10}(N) = -73.979 \text{ dB} + 18.062 \text{ dB} = -55.92 \text{ dB}$$

$$SSB_{input} = 20 \log_{10} \left(\frac{\theta_d}{2} \right) \quad \rightarrow \quad \theta_d = 2 \cdot 10^{SSB_{input}/20} = \underline{0.0032 \text{ radians}}$$

Problem 5 – (10 points)

On page 200-16 of the lecture notes, the illustration of how a rotational frequency detector works is given. Use this diagram to clearly explain how the rotational frequency detector works.

Solution

Rotational Frequency Detector

When referenceless frequency acquisition is desired for CDR applications, a frequency detector as shown below can be used in a frequency locked loop for pulling the VCO frequency to the correct data rate. Once, the VCO frequency is centered to corresponding data rate, the phase locking loop takes over in order to sample the data at optimum sampling point.

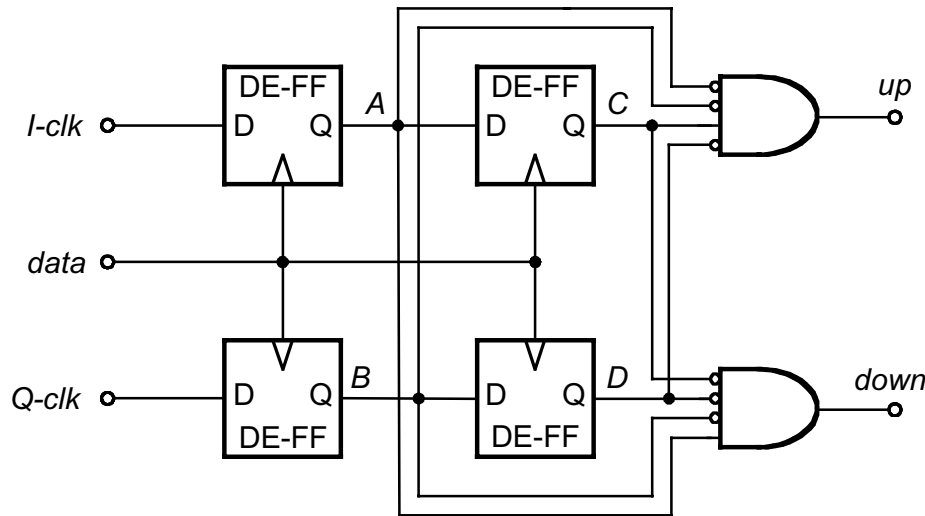


Figure 1: Rotational frequency detector. I and Q clocks come from the VCO. Data is the non-return to zero (NRZ) data to be resampled by the clock and data recovery circuit (CDR). The flip flops are double edge sampling FFs. States A and B hold the present sampled I and Q clocks whereas the C and D hold the previously sampled inputs (A and B are resampled) UP is 1 when AB CD = 00 10. DOWN is 1 when AB CD = 10 00.

A typical frequency detector waveform for data slower than VCO clock is shown below. Note that, anytime when AB changes from 00 to 10 a DOWN pulse is generated. In this example, there is no UP pulse since no 10 to 00 transition occurs.

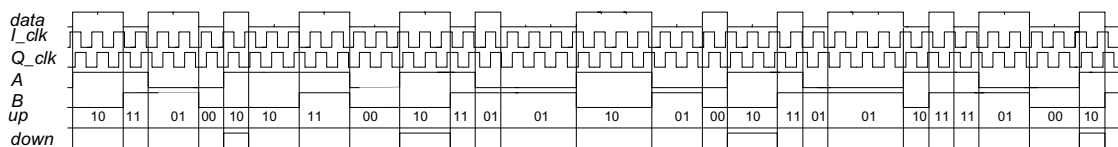


Figure 2: Typical FD waveform example.

In figure below, the I and Q VCO clocks are 12.5% faster than the incoming sampling clock. As a result, the beat frequency (frequency offset between VCO and sampling clocks) vector shown, takes 8 samples in counterclockwise direction to come to its initial position. Initially, the sampling clock is sampling I and Q clocks when I is low and Q is high (01). Next time, it samples IQ=01 one more time. Next two times, it samples 00. The next sampling result is 10. The decision point is 00 to 10 transition or 10 to 00 transition. In the former one, a DOWN signal is produced and in the later case an UP pulse is produced. During the entire beat period (i.e., 8 samples) only one down pulse is produced).

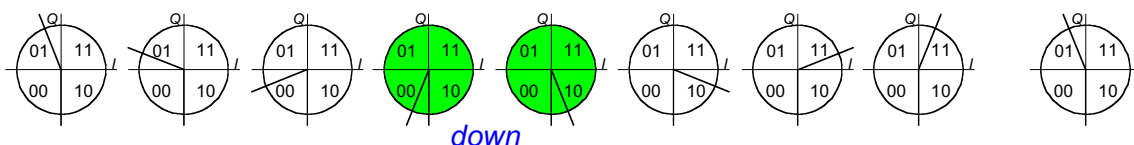


Figure 3: IQ clocks are 12.5% faster than sampling clock.

In the example below, VCO clock is 25% faster. Therefore, the beat frequency completes its full rotation in 4 cycles. In 8 cycles there are two 00 to 10 transitions or equivalently two DOWN pulses are produced by the frequency detector.

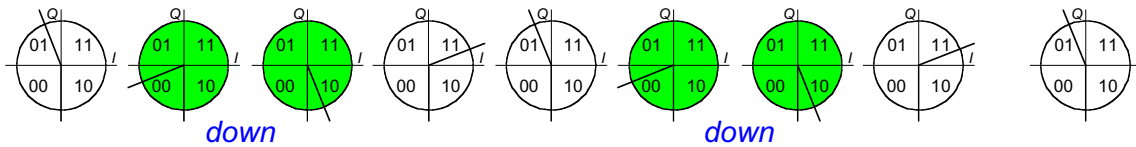


Figure 4: IQ clocks are 25.0% faster than sampling clock.

Now, let's look at what happens if the VCO clock is 37.5% faster than the sampling clock. The beat frequency rotation vector comes to its starting position in 8 cycles, and during which only one 00 to 10 transition is made. Note that from the 4th position to 5th position, the beat frequency vector, skip the quadrant 00. Therefore, the past state of the sampling state CD and present sampling state AB which goes to the four input AND signals are 01 and 10. As a result, both outputs remain at 0. No UP and DOWN generated when one of the decision quadrants are skipped.

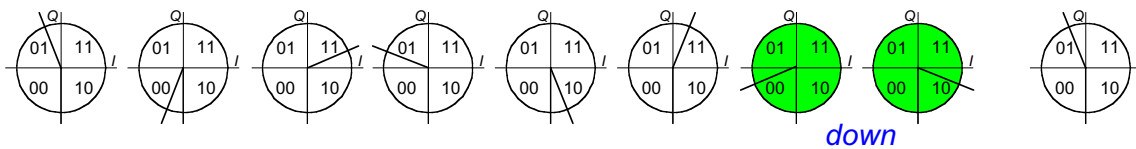


Figure 5: IQ clocks are 37.5% faster than sampling clock.

When the speed difference is 50%, there is no 00 to 10 transition. As a result no UP/DOWN pulses generated.

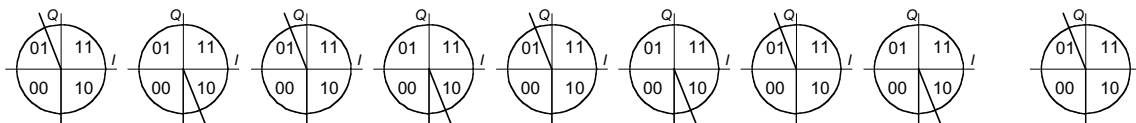


Figure 6: IQ clocks are 50% faster (or slower) than sampling clock.

The case where VCO is 62.5% percent faster than the sampling clock: During the 8 sampling period in which the beat frequency vector comes to its initial starting point, there is only one transition between quadrants 3 and 4. This transition, however is on the reverse direction. That is CD=10 to AB=00. The AND gates in this case generate an UP pulse. To the frequency detector, VCO appears to be 37.5% slower instead of 62.5% faster. A wrong pulse is generated.

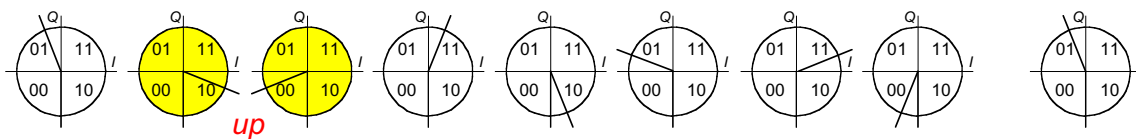


Figure 7: IQ clocks are 50% faster (frequency detector interprets this as VCO is 37.5% slower) than sampling clock.

The above examples is for the case when VCO is faster. The case in which the VCO is slower can be plotted similarly. When VCO is slow, the beat frequency vector traverses the IQ quadrant planes in clockwise direction. In the light of above vector diagrams, the following frequency detector output vs. frequency input waveform can be plotted.

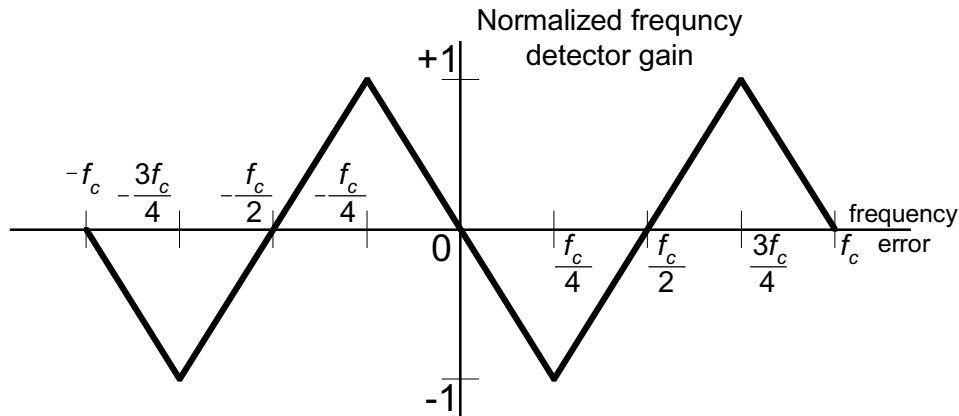


Figure 8: Frequency detector characteristics when the sampling input is clock instead of NRZ data.

Note that, the pulling range of this frequency detector is +/-50% when a full rate clock signal is rising (or falling) edge samples the I and Q VCO clocks, instead of data sampling the I and Q clocks at both rising and falling edges. This case is explained below.

From Figure 8, the detector gain is maximum for +/-25% frequency offset. (Two DOWN pulses in Figure 4 above). Above +/-50% frequency offset, the output changes polarity and VCO frequency is pulled to the wrong direction. The useful range is, therefore only +/-50%.

The above phase diagram example is for the case if the frequency detector input is a full-rate clock instead of NRZ data. We further assumed that, I and Q clocks are sampled only at one edge of the clock (either rising or falling). A pseudo random NRZ data resembles to a clock with 1/4th of the full speed clock as far as the transition density is concerned. If this fact is combined with the double edge sampling nature of the actual frequency detector, the data sampling the I and Q clocks can be assumed as half the full speed clock. That is, in above phasor diagrams, the IQ clocks are effectively sampled every other time. In this case, the frequency detector characteristics, changes polarity when VCO range exceeds +/-25% of the data rate. For actual data inputs, therefore the frequency characteristics resembles to the following figure. The rounded edges of the gain characteristics is due to the pseudo random nature of the input bit sequence (PRBS).

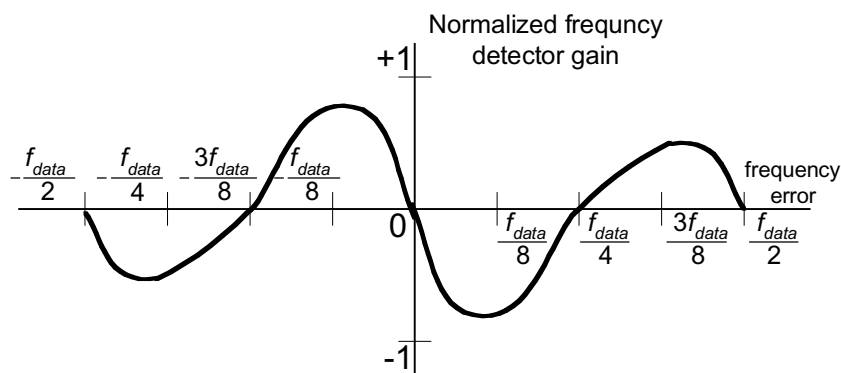


Figure 10: Rotational frequency detector characteristics for PRBS NRZ data.