LECTURE 030 – INTEGRATED CIRCUIT TECHNOLOGY - I

(References – [7,8])

Objective

The objective of this presentation is:

1.) Illustrate integrated circuit technology suitable for frequency synthesizers

2.) Provide a background for understanding integrated passive components

Outline

- Introduction
- CMOS Technology
- BiCMOS Technology
- Summary

INTRODUCTION

Classification of Silicon Technology

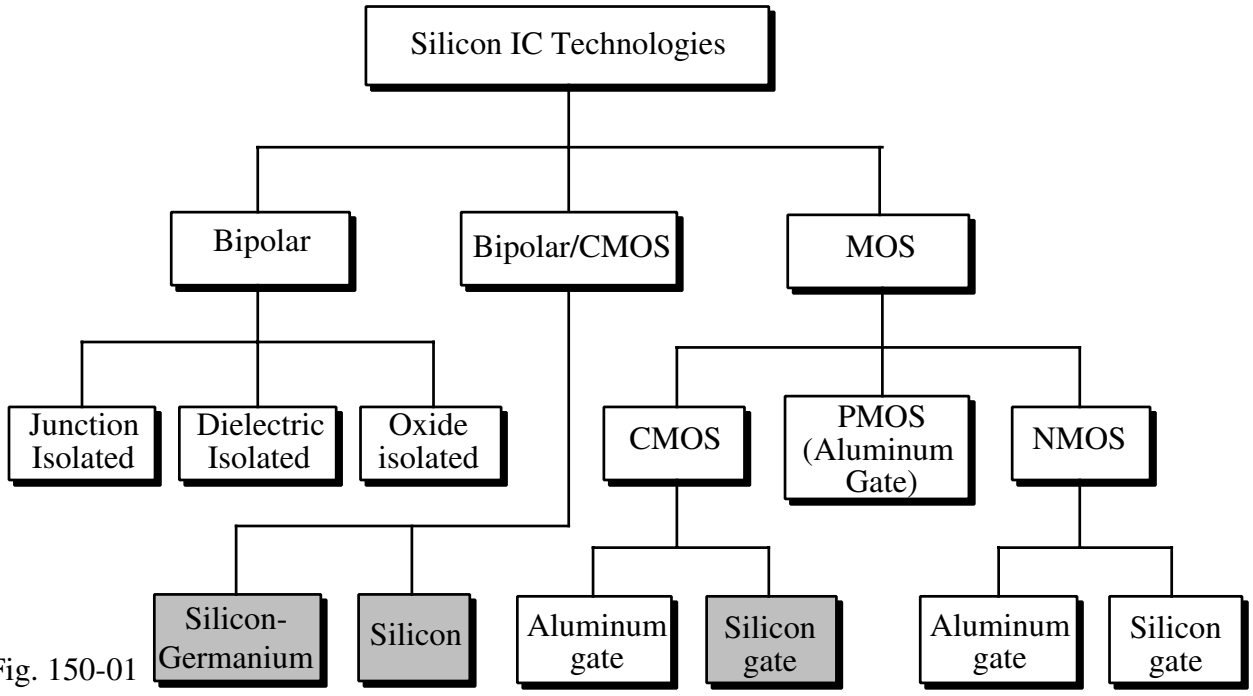


Fig. 150-01

Why CMOS Technology?

Comparison of BJT and MOSFET technology from an analog viewpoint:

Feature	BJT	MOSFET
Cutoff Frequency(f_T)	100 GHz	50 GHz (0.25μm)
Noise (thermal about the same)	Less 1/f	More 1/f
DC Range of Operation	9 decades of exponential current versus v_{BE}	2-3 decades of square law behavior
Small Signal Output Resistance	Slightly larger	Smaller for short channel
Switch Implementation	Poor	Good
Capacitor Implementation	Voltage dependent	Reasonably good

Therefore,

- Almost every comparison favors the BJT, *however* a similar comparison made from a digital viewpoint would come up on the side of CMOS.
- Therefore, since large-volume technology will be driven by digital demands, CMOS is an obvious result as the technology of availability.

Other factors:

- The potential for technology improvement for CMOS is greater than for BJT
- Performance generally increases with decreasing channel length

Components of a Modern CMOS Technology

Illustration of a modern CMOS process:

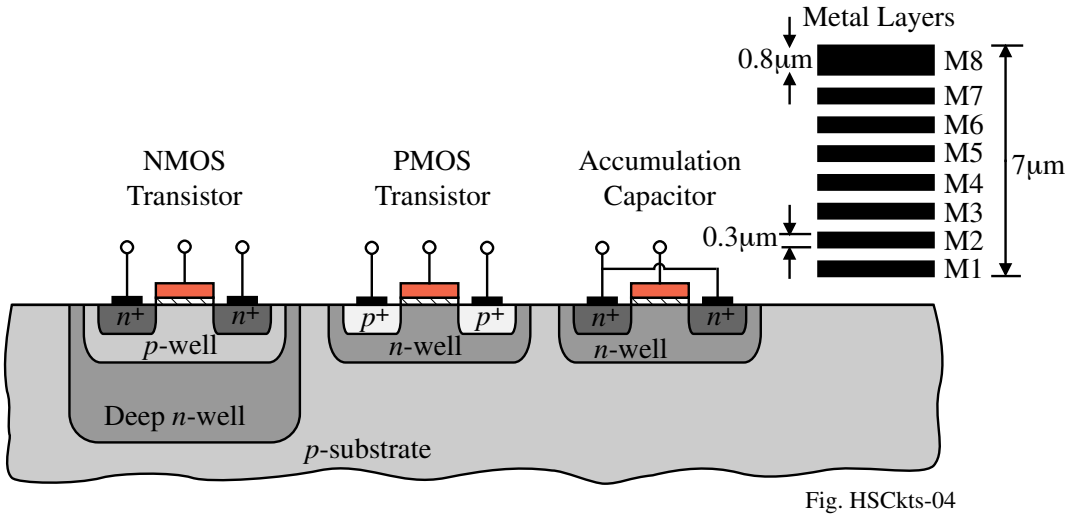


Fig. HSCkts-04

In addition to NMOS and PMOS transistors, the technology provides:

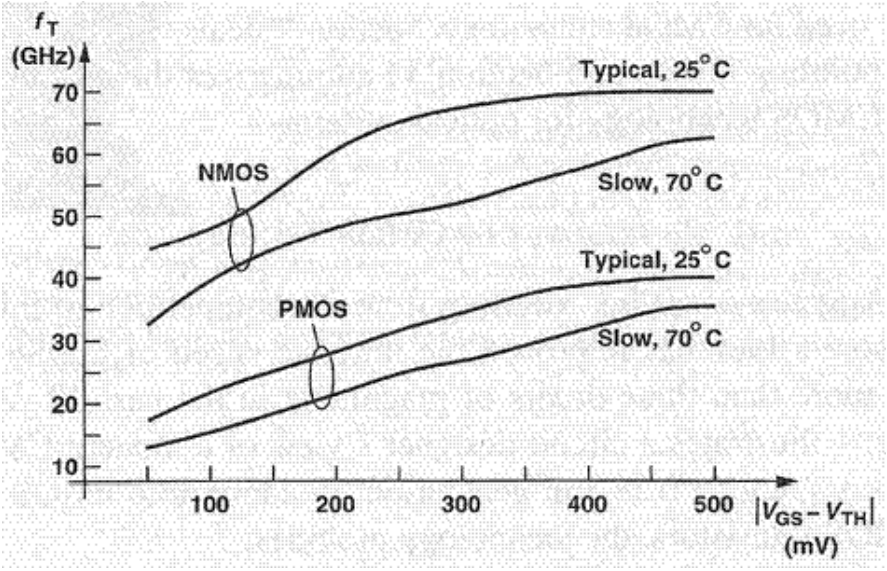
1.) A deep *n*-well that can be utilized to reduce substrate noise coupling.

2.) A MOS varactor that can serve in VCOs

3.) At least 6 levels of metal that can form many useful structures such as inductors, capacitors, and transmission lines.

CMOS Components – Transistors

f_T as a function of gate-source overdrive, V_{GS}-V_T (0.13μm):



The upper frequency limit is probably around 40 GHz for NMOS with an f_T in the vicinity of 60GHz with an overdrive of 0.5V and at the slow-high temperature corner.

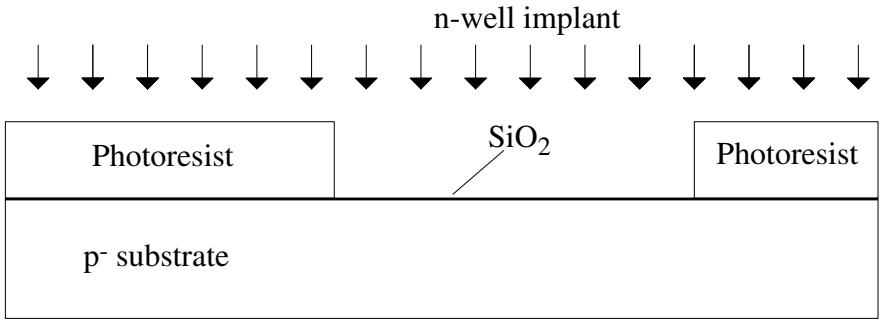
TYPICAL CMOS FABRICATION PROCESS

N-Well CMOS Fabrication Major Steps

1.) Implant and diffuse the n-well
2.) Deposition of silicon nitride
3.) n-type field (channel stop) implant
4.) p-type field (channel stop) implant
5.) Grow a thick field oxide (FOX)
6.) Grow a thin oxide and deposit polysilicon
7.) Remove poly and form LDD spacers
8.) Implantation of NMOS S/D and n-material contacts
9.) Remove spacers and implant NMOS LDDs
10.) Repeat steps 8.) and 9.) for PMOS
11.) Anneal to activate the implanted ions
12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)
13.) Open contacts, deposit first level metal and etch unwanted metal
14.) Deposit another interlayer dielectric (CVD SiO_2), open vias, deposit 2nd level metal
15.) Etch unwanted metal, deposit a passivation layer and open over bonding pads

Major CMOS Process Steps

Step 1 - Implantation and diffusion of the n-wells



Step 2 - Growth of thin oxide and deposition of silicon nitride

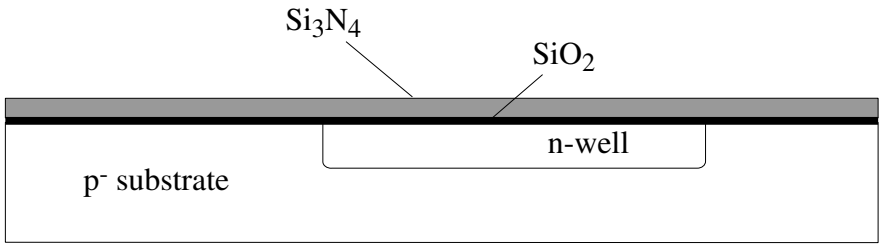
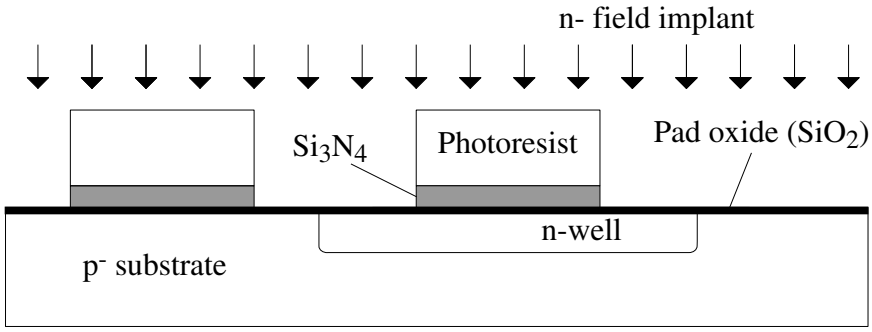


Fig. 180-01

Major CMOS Process Steps - Continued

Step 3.) Implantation of the n-type field channel stop



Step 4.) Implantation of the p-type field channel stop

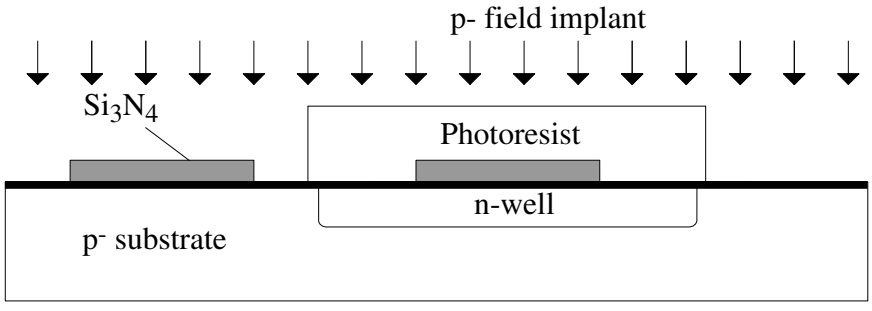
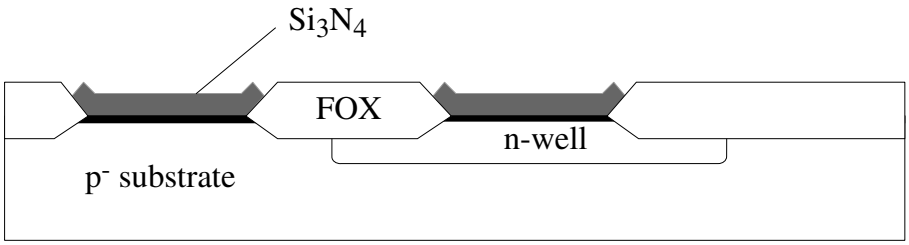


Fig. 180-02

Major CMOS Process Steps – Continued

Step 5.) Growth of the thick field oxide (LOCOS - *loc*alized *o*xidation of *s*ilicon)



Step 6.) Growth of the gate thin oxide and deposition of polysilicon. The thresholds can be shifted by an implantation before the deposition of polysilicon.

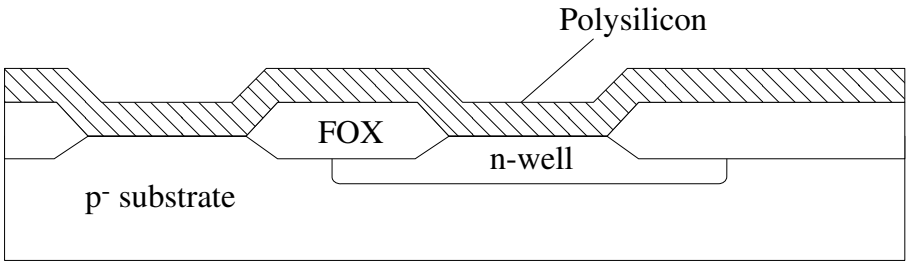
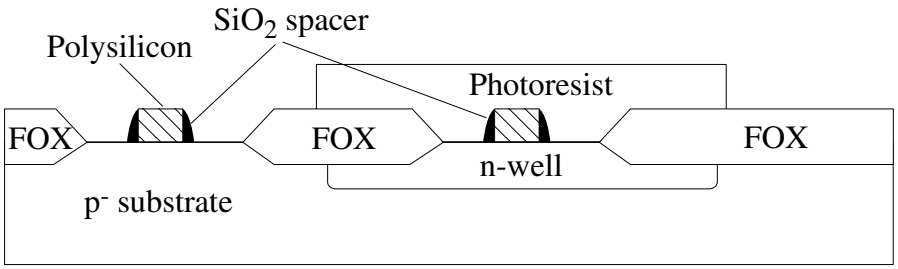


Fig. 180-03

Major CMOS Process Steps - Continued

Step 7.) Removal of polysilicon and formation of the sidewall spacers



Step 8.) Implantation of NMOS source and drain and contact to n-well (not shown)

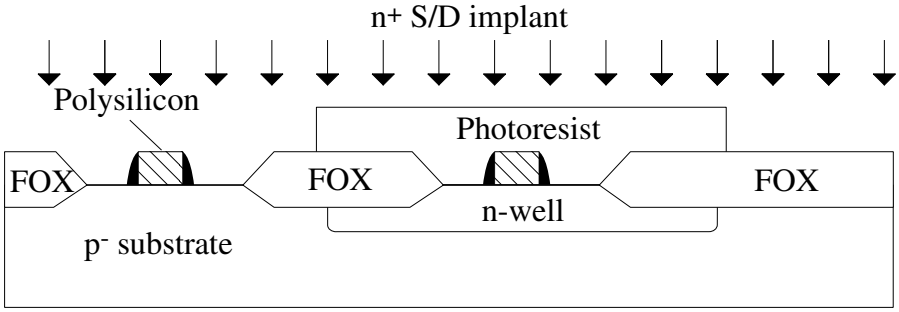
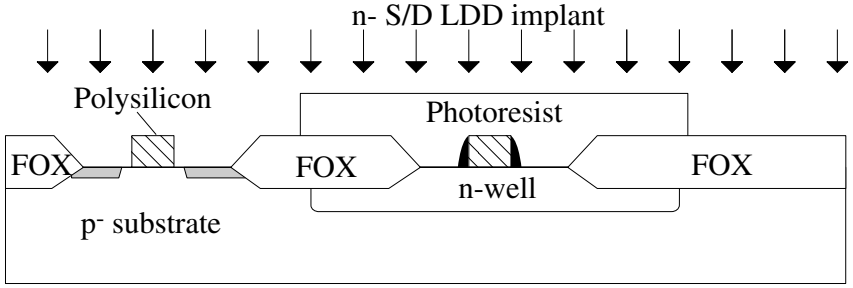


Fig. 180-04

Major CMOS Process Steps - Continued

Step 9.) Remove sidewall spacers and implant the NMOS lightly doped source/drains



Step 10.) Implant the PMOS source/drains and contacts to the p- substrate (not shown), remove the sidewall spacers and implant the PMOS lightly doped source/drains

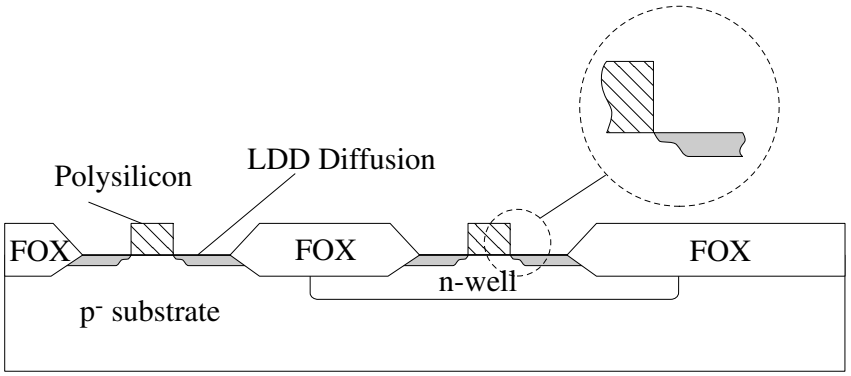
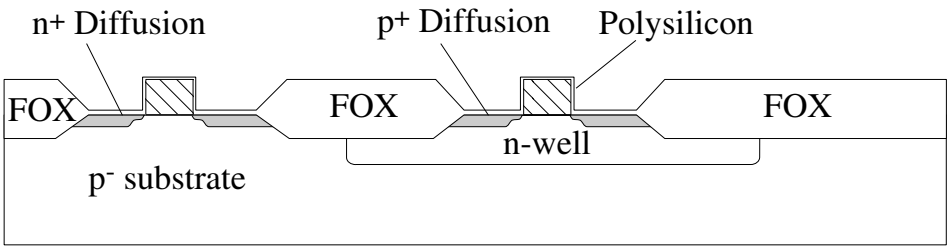


Fig. 180-05

Major CMOS Process Steps – Continued

Step 11.) Anneal to activate the implanted ions



Step 12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)

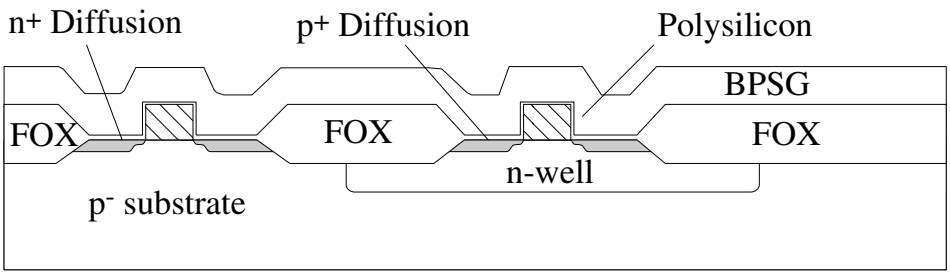
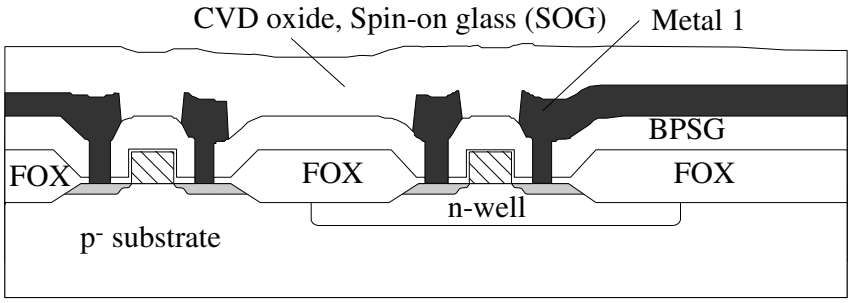


Fig. 180-06

Major CMOS Process Steps - Continued

Step 13.) Open contacts, deposit first level metal and etch unwanted metal



Step 14.) Deposit another interlayer dielectric (CVD SiO_2), open contacts, deposit second level metall

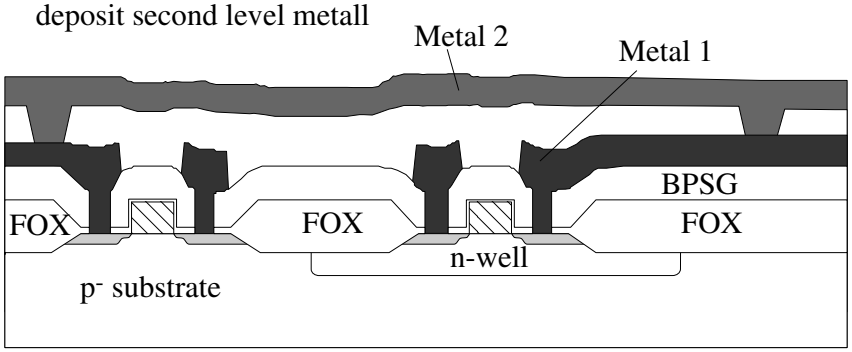


Fig. 180-07

Major CMOS Process Steps – Continued

Step 15.) Etch unwanted metal and deposit a passivation layer and open over bonding pads

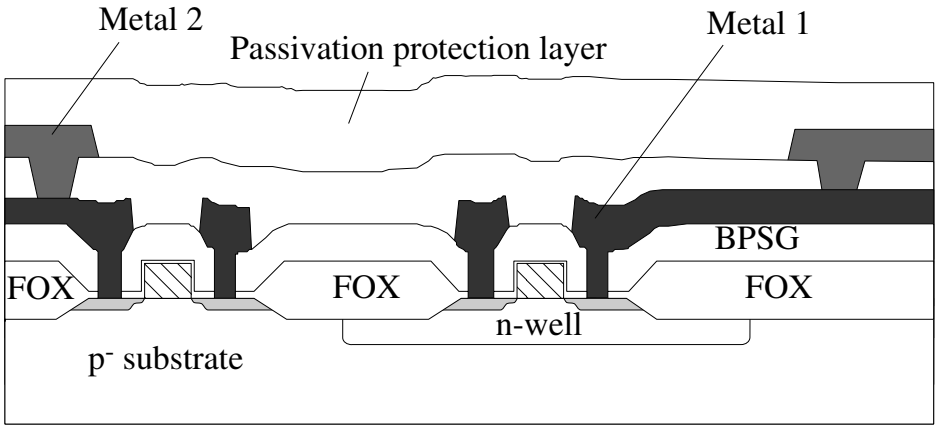


Fig. 180-08

p-well process is similar but starts with a p-well implant rather than an n-well implant.

Approximate Side View of CMOS Fabrication

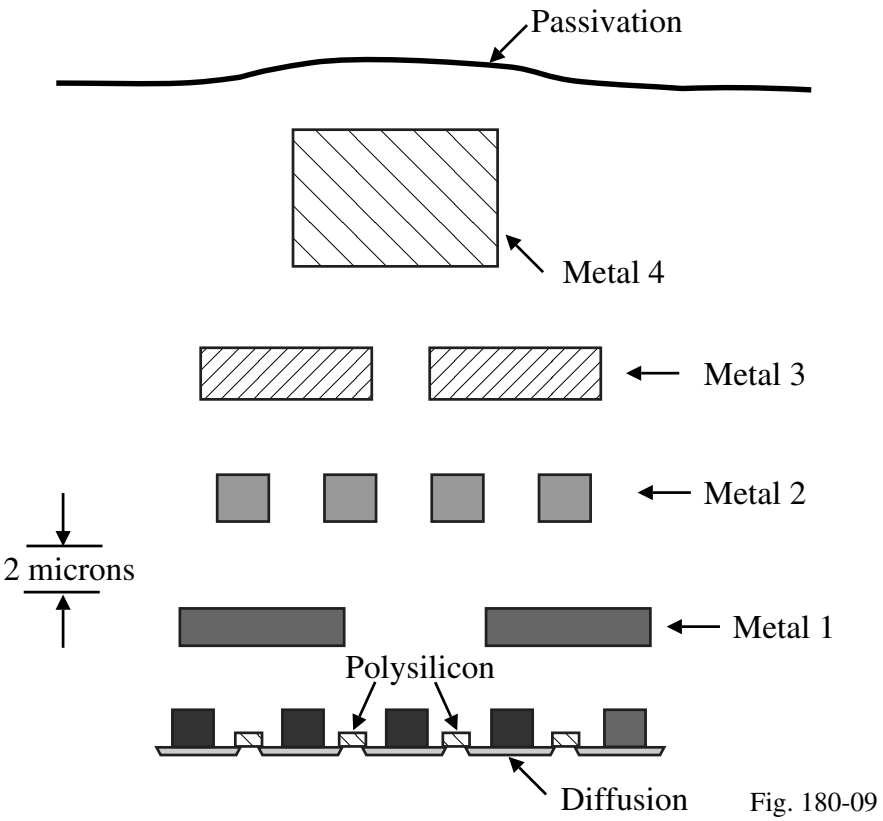
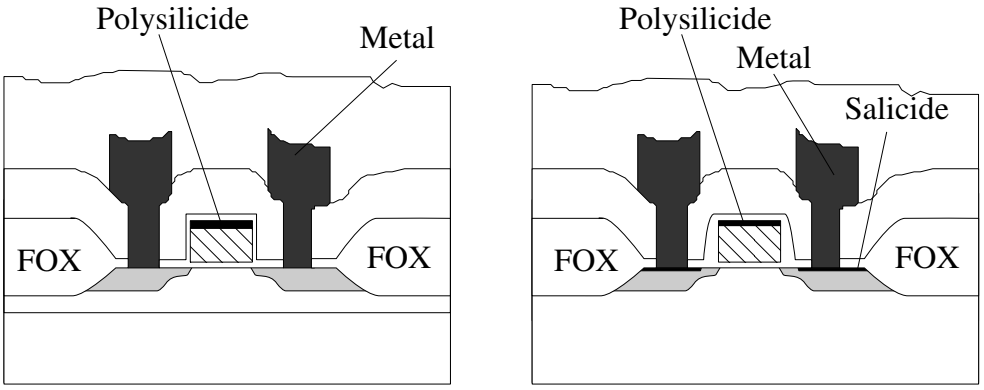


Fig. 180-09

Silicide/Salicide Technology

Used to reduce interconnect resistivity by placing a low-resistance silicide such as $TiSi_2$, WSi_2, $TaSi_2$, etc. on top of polysilicon

Salicide technology (self-aligned silicide) provides low resistance source/drain connections as well as low-resistance polysilicon.



Polycide structure Salicide structure

Fig 180-10

Scanning Electron Microscope of a MOSFET Cross-section

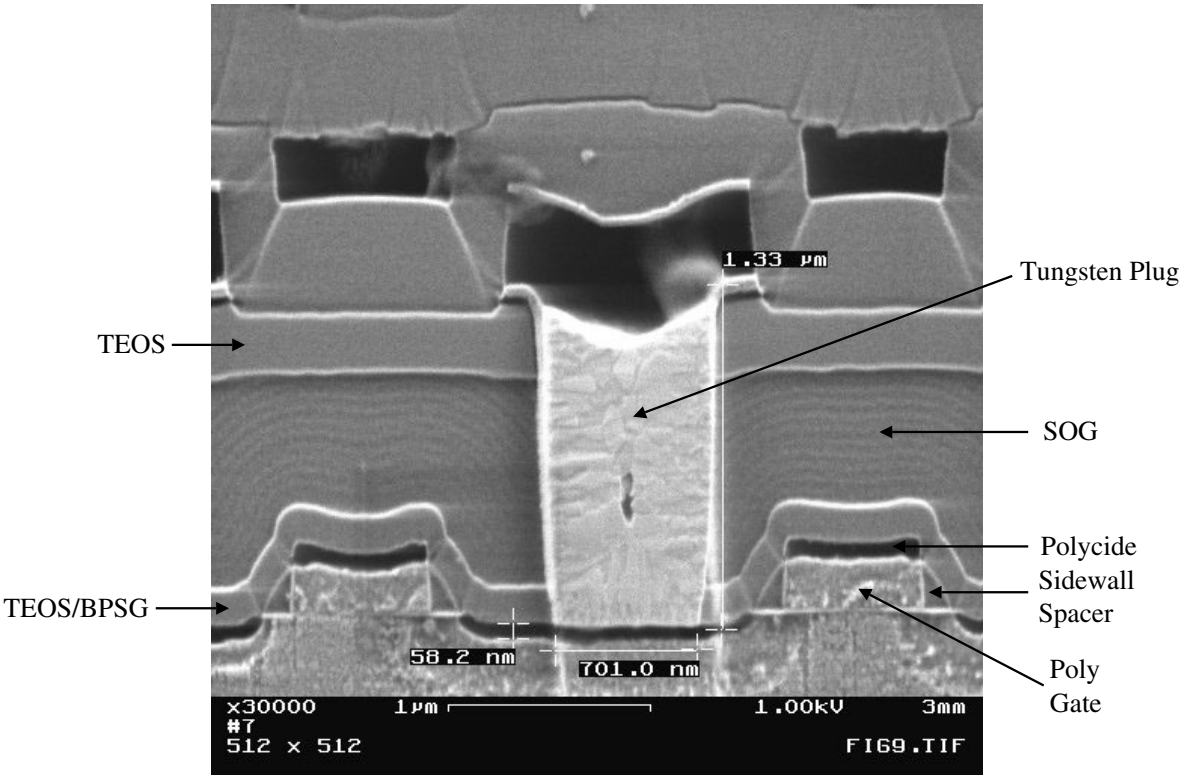


Fig. 2.8-20

Scanning Electron Microscope Showing Metal Levels and Interconnect

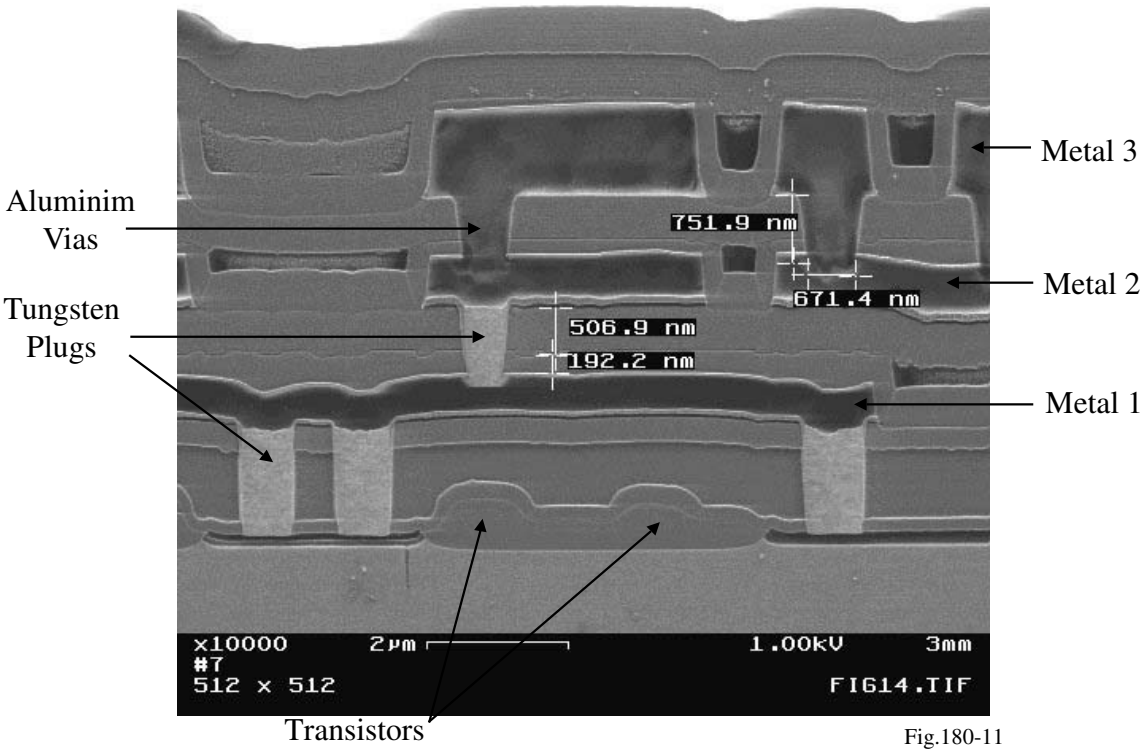


Fig.180-11

BiCMOS TECHNOLOGY

Typical 0.5μm BiCMOS Technology

Masking Sequence:

1. Buried n^+ layer
2. Buried p^+ layer
3. Collector tub
4. Active area
5. Collector sinker
6. n-well
7. p-well
8. Emitter window
9. Base oxide/implant
10. Emitter implant
11. Poly 1
12. NMOS lightly doped drain
13. PMOS lightly doped drain
14. n^+ source/drain
15. p^+ source/drain
16. Silicide protection
17. Contacts
18. Metal 1
19. Via 1
20. Metal 2
21. Via 2
22. Metal 3
23. Nitride passivation

Notation:

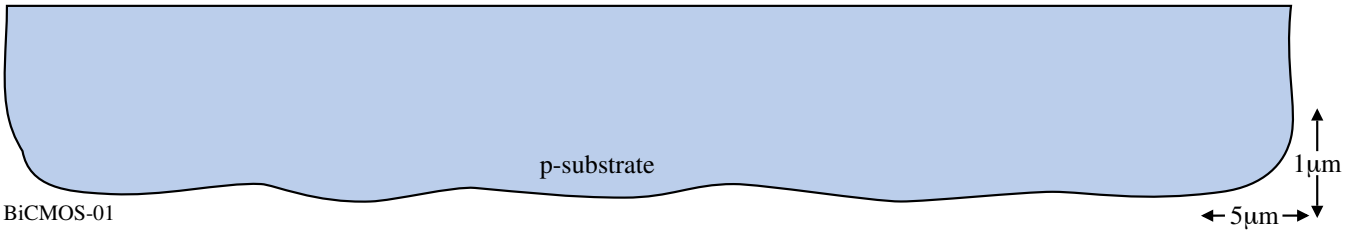
BSPG = Boron and Phosphorus doped Silicate Glass (oxide)

Kooi Nitride = A thin layer of silicon nitride on the silicon surface as a result of the reaction of silicon with the HN3 generated, during the field oxidation.

TEOS = Tetro-Ethyl-Ortho-Silicate. A chemical compound used to deposit conformal oxide films.

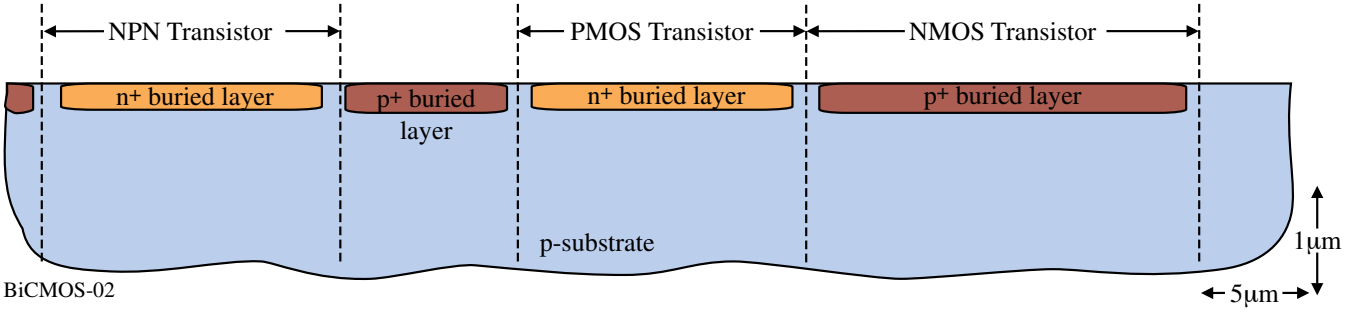
n^+ and p^+ Buried Layers

Starting Substrate:



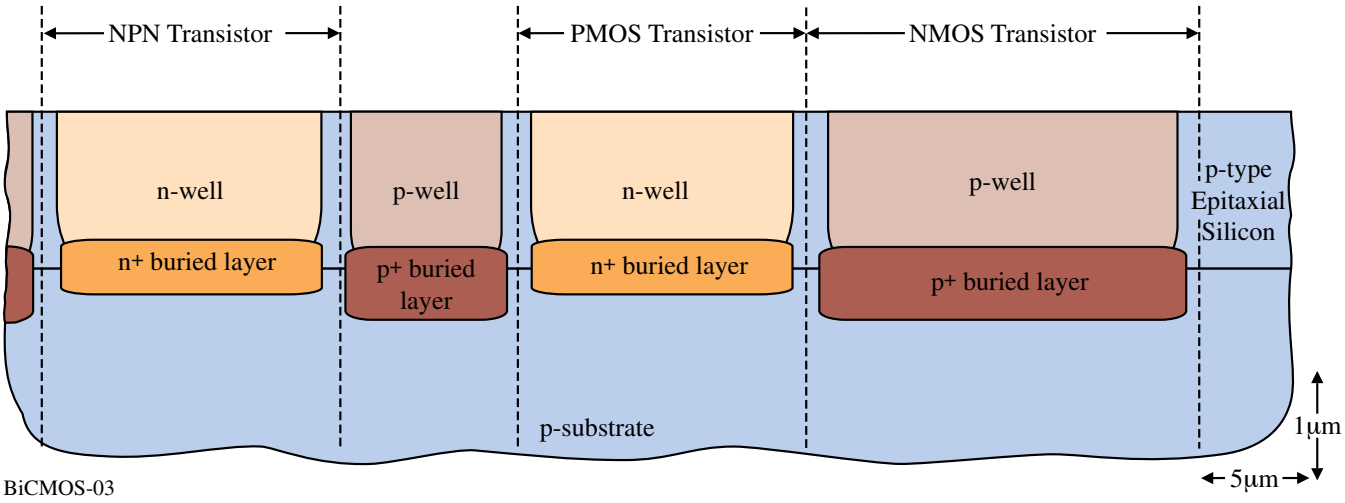
BiCMOS-01

n^+ and p^+ Buried Layers:



BiCMOS-02

Epitaxial Growth

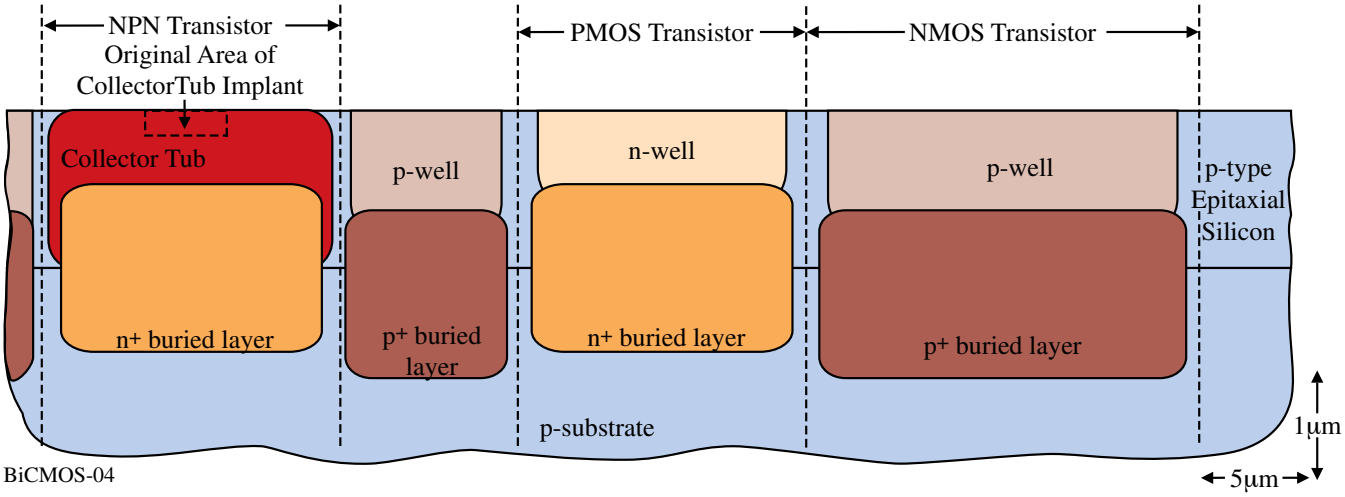


BiCMOS-03

Comment:

- As the epi layer grows vertically, it assumes the doping level of the substrate beneath it.
- In addition, the high temperature of the epitaxial process causes the buried layers to diffuse upward and downward.

Collector Tub

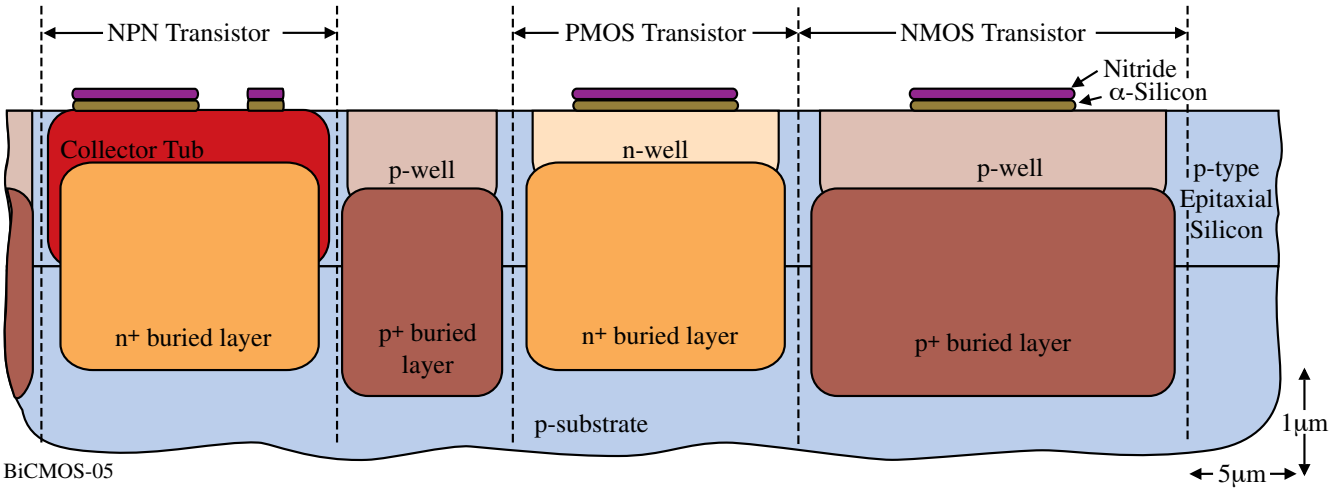


BiCMOS-04

Comment:

- The collector area is developed by an initial implant followed by a drive-in diffusion to form the collector tub.

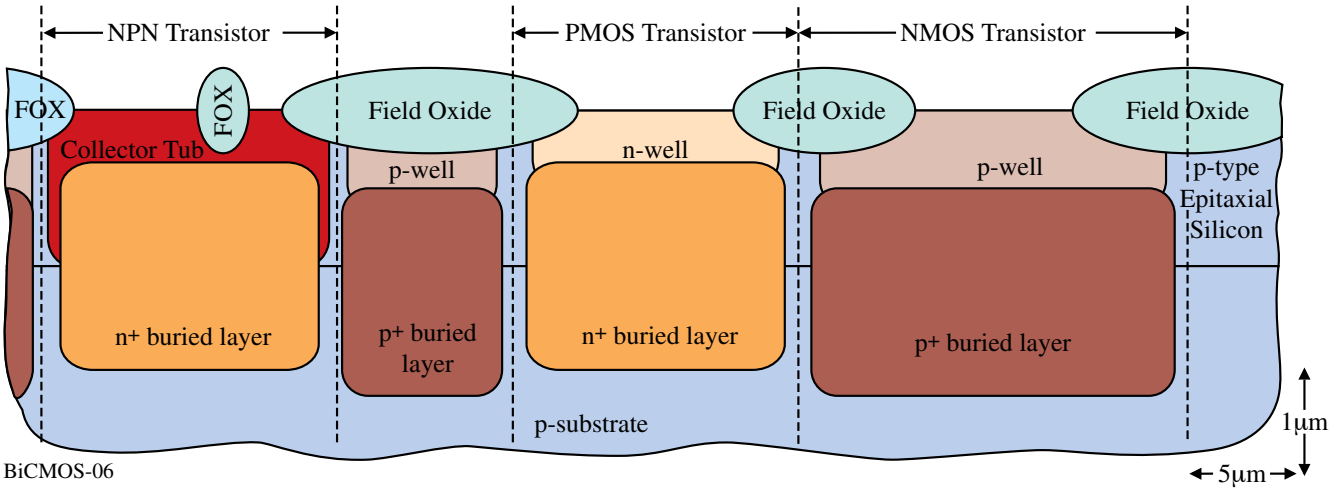
Active Area Definition



Comment:

- The silicon nitride is use to impede the growth of the thick oxide which allows contact to the substrate
- α-silicon is used for stress relief and to minimize the bird's beak encroachment

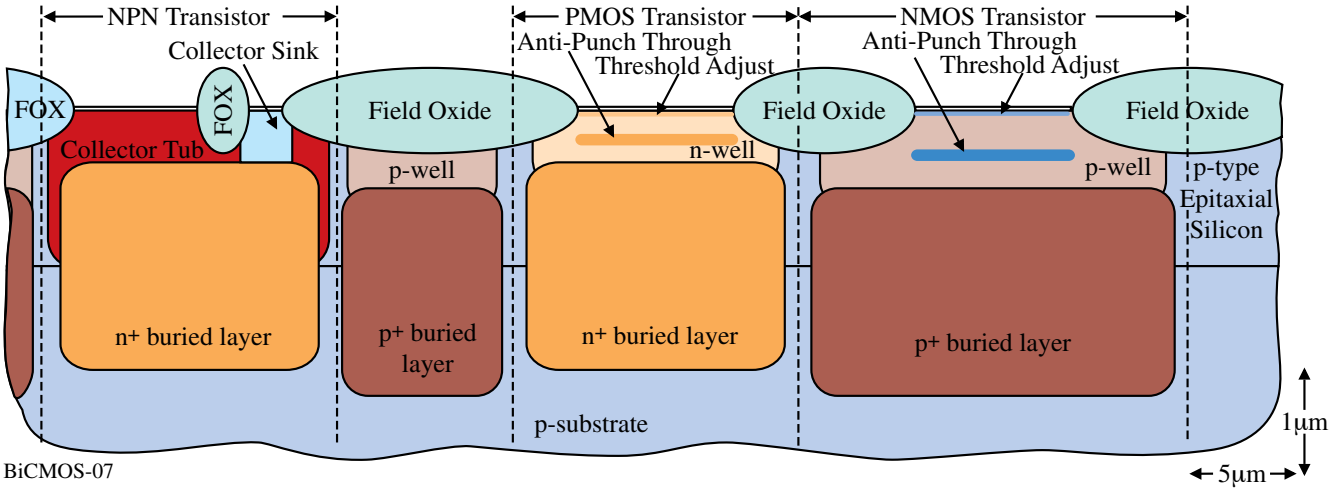
Field Oxide



Comments:

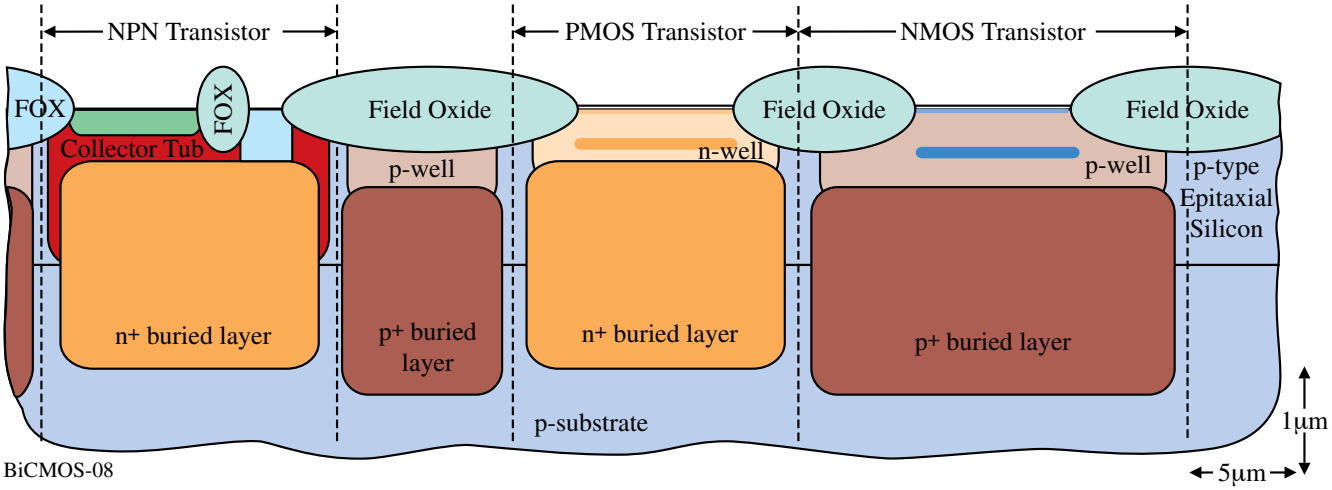
- The field oxide is used to isolate surface structures (i.e. metal) from the substrate

Collector Sink and n-Well and p-Well Definitions



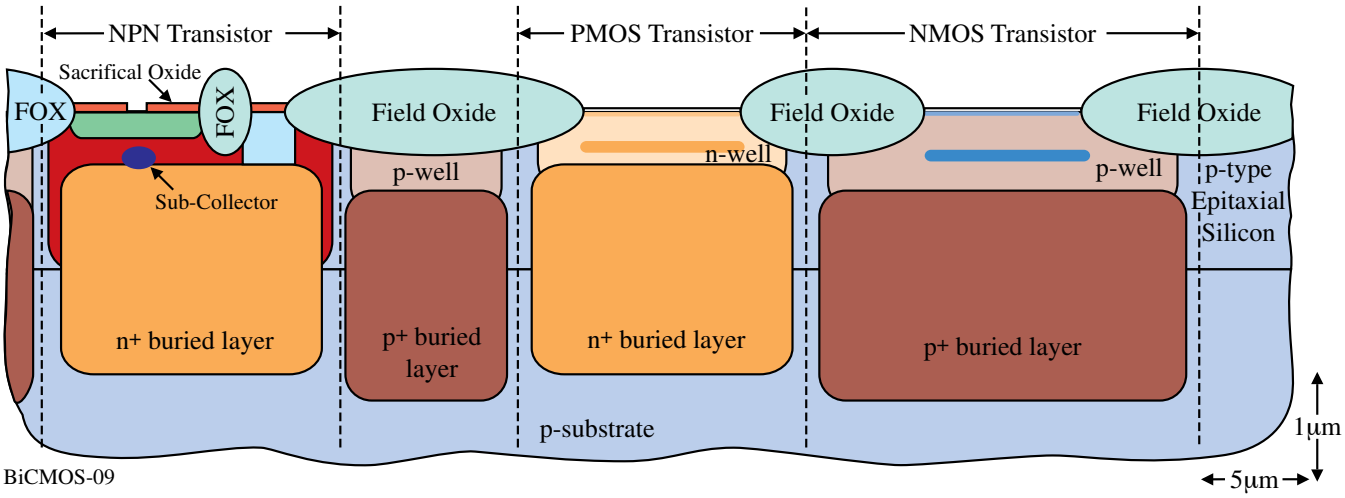
BiCMOS-07

Base Definition

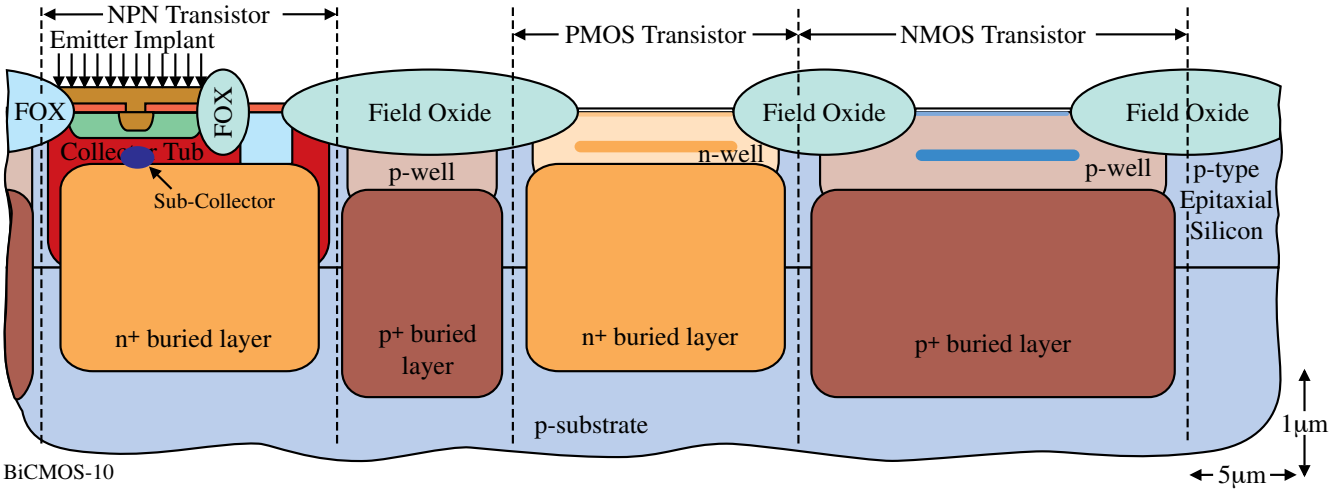


BiCMOS-08

Definition of the Emitter Window and Sub-Collector Implant



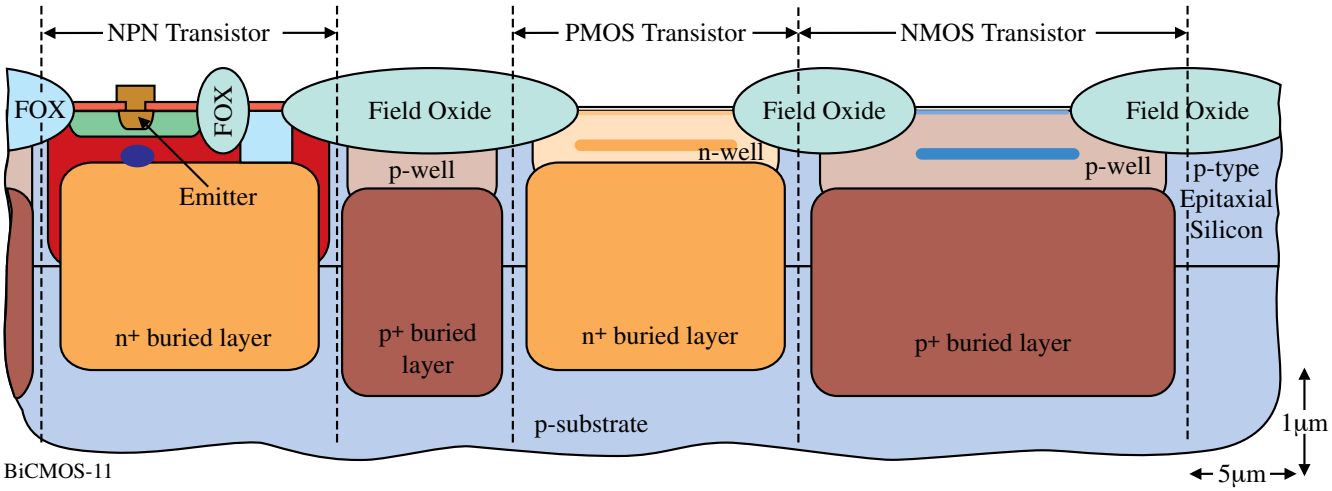
Emitter Implant



Comments:

- The polysilicon above the base is implanted with n-type carriers

Emitter Diffusion

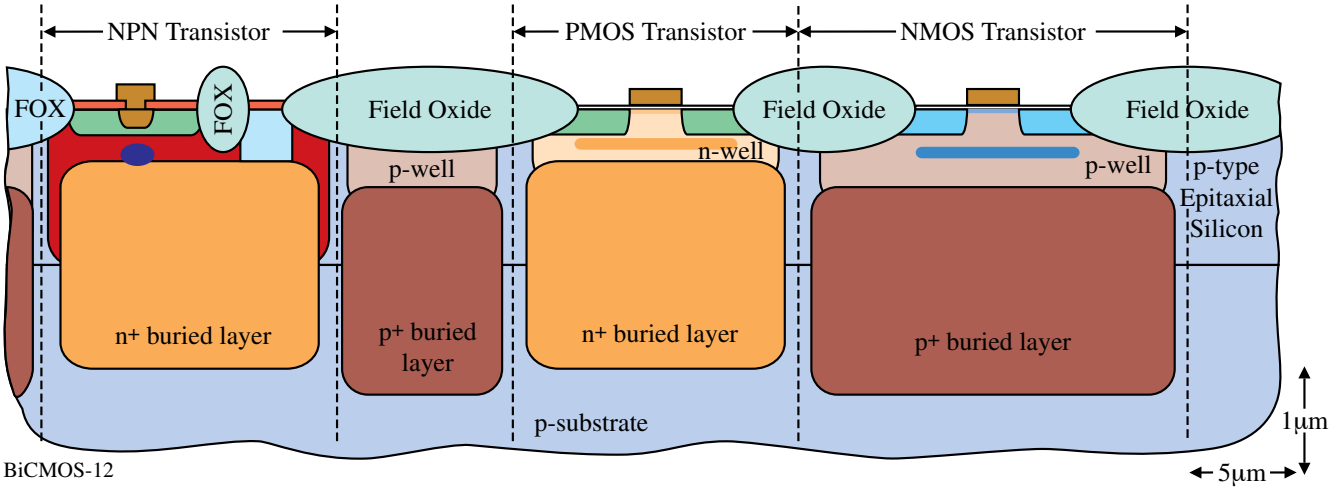


BiCMOS-11

Comments:

- The polysilicon not over the emitter window is removed and the n-type carriers diffuse into the base forming the emitter

Formation of the MOS Gates and LD Drains/Sources

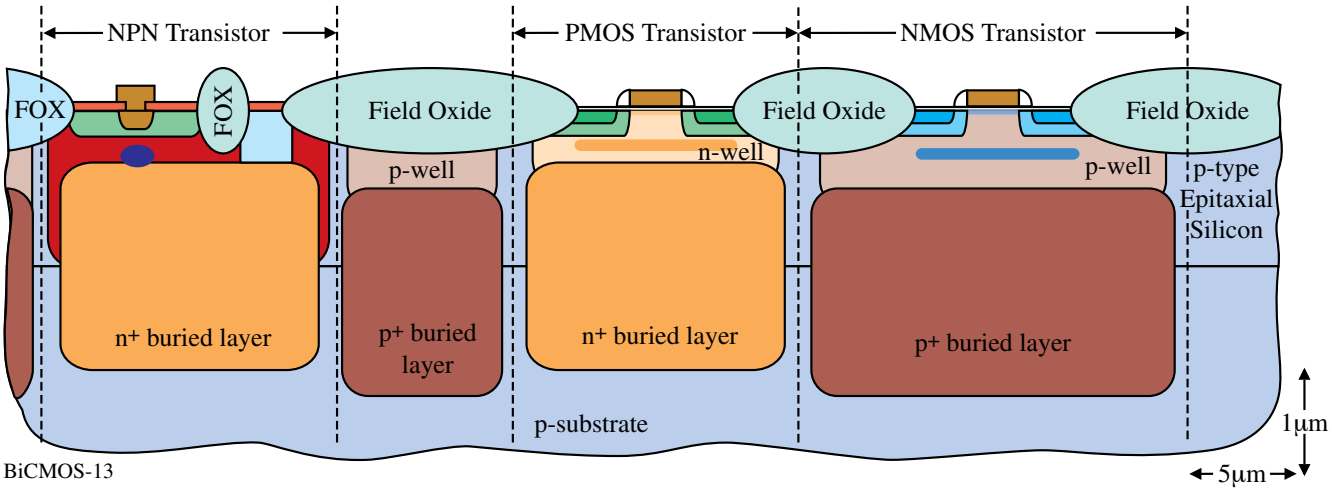


BiCMOS-12

Comments:

- The surface of the region where the MOSFETs are to be built is cleared and a thin gate oxide is deposited with a polysilicon layer on top of the thin oxide
- The polysilicon is removed over the source and drain areas
- A light source/drain diffusion is done for the NMOS and PMOS (separately)

Heavily Doped Source/Drain

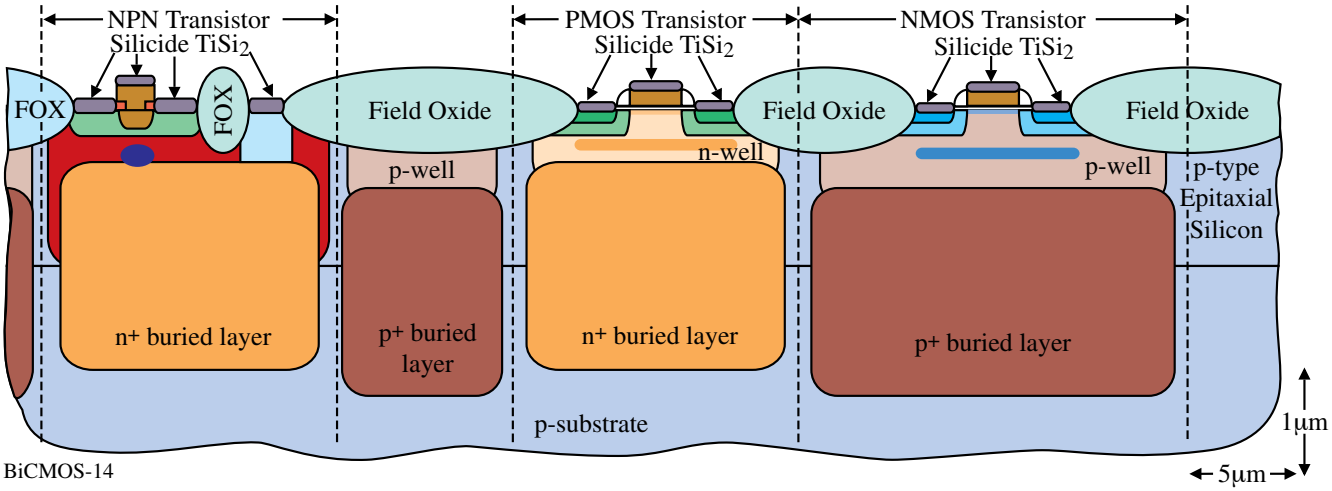


BiCMOS-13

Comments:

- The sidewall spacers prevent the heavy source/drain doping from being near the channel of the MOSFET

Siliciding

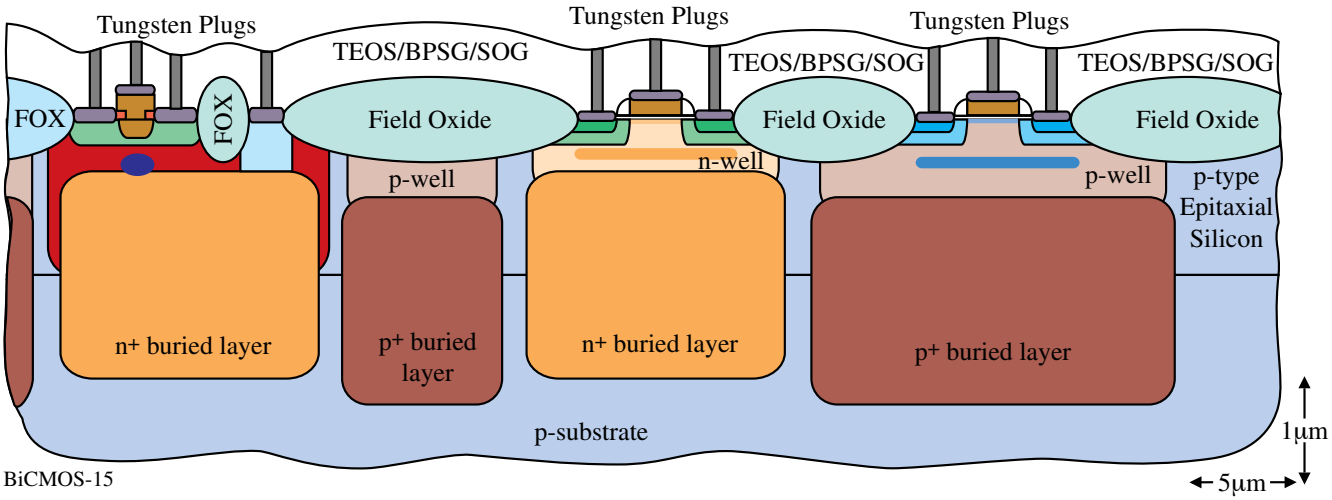


BiCMOS-14

Comments:

- Siliciding is used to reduce the resistance of the polysilicon and to provide ohmic contacts to the base, emitter, collector, sources and drains

Contacts

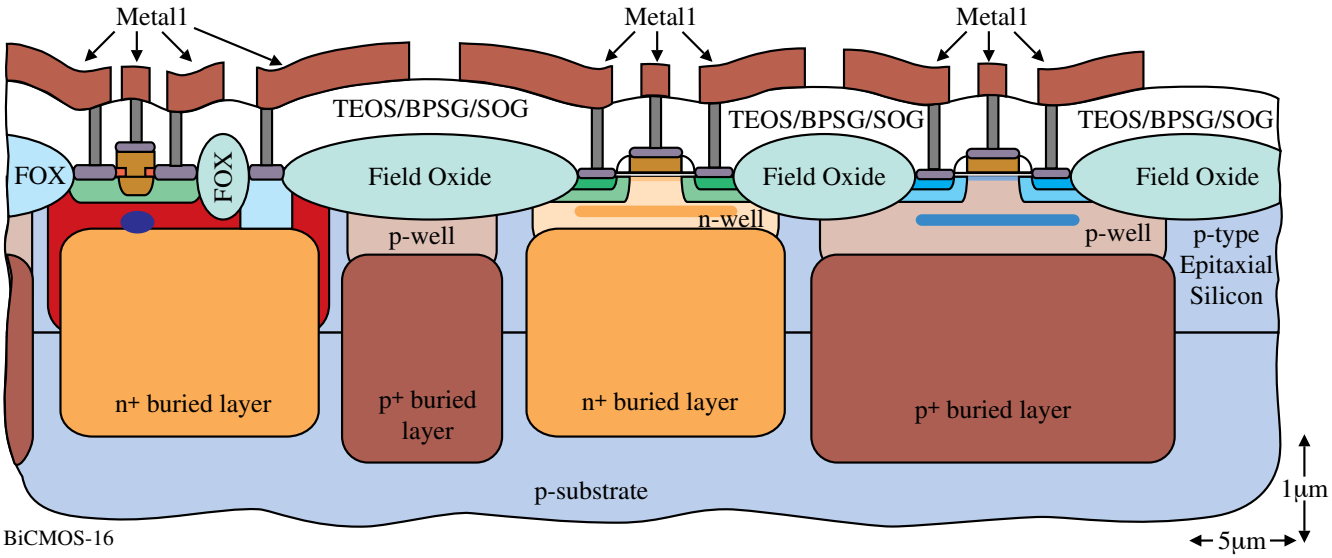


BiCMOS-15

Comments:

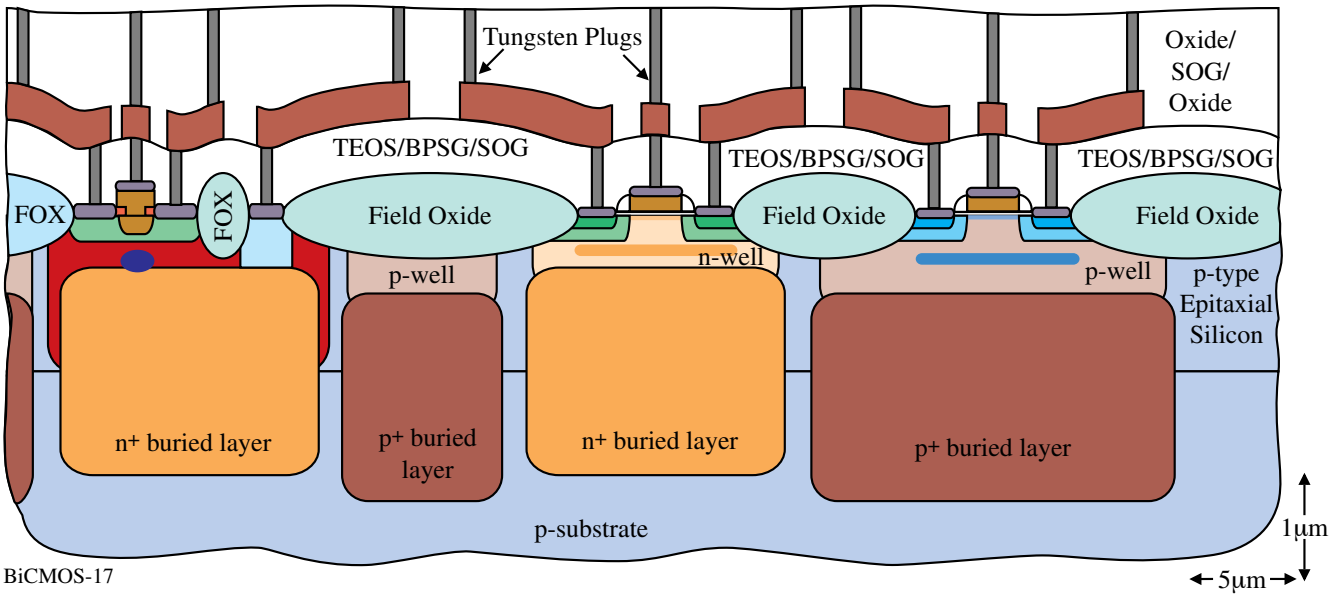
- A dielectric is deposited over the entire wafer
- One of the purposes of the dielectric is to smooth out the surface
- Tungsten plugs are used to make electrical contact between the transistors and metal1

Metal1



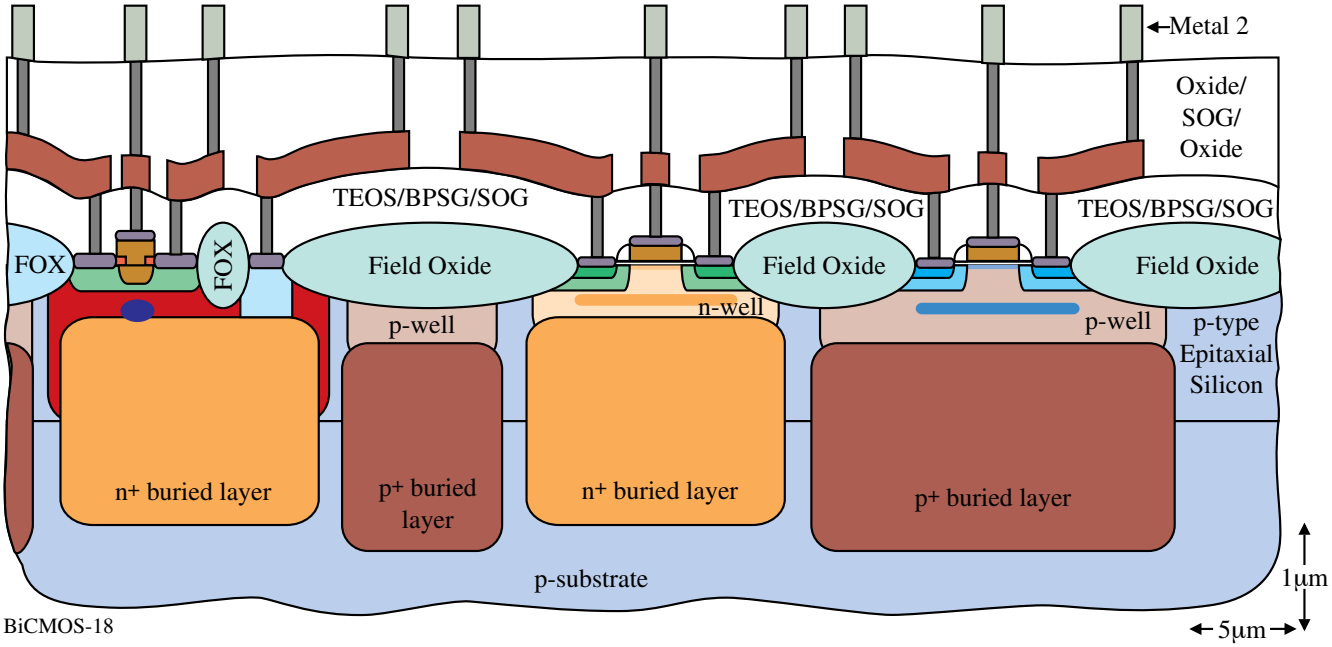
BiCMOS-16

Metal1-Metal2 Vias



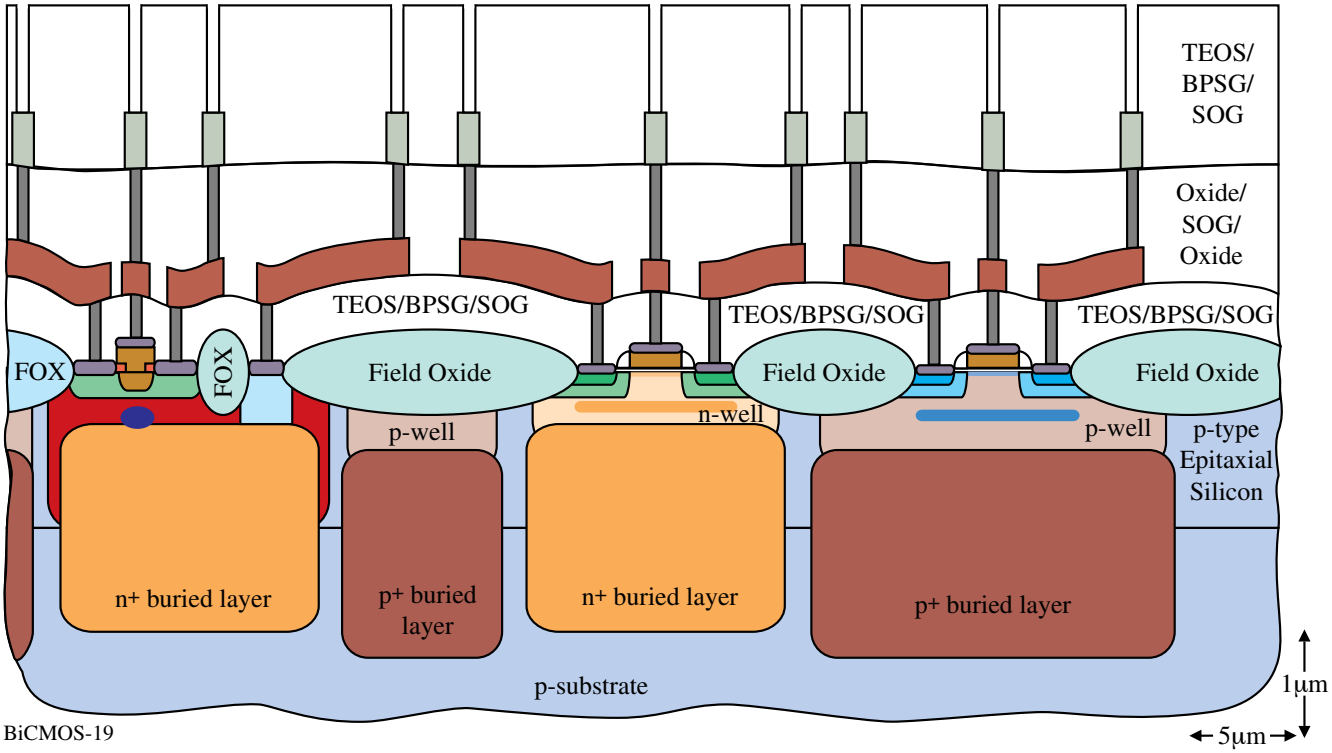
BiCMOS-17

Metal2



BiCMOS-18

Metal2-Metal3 Vias

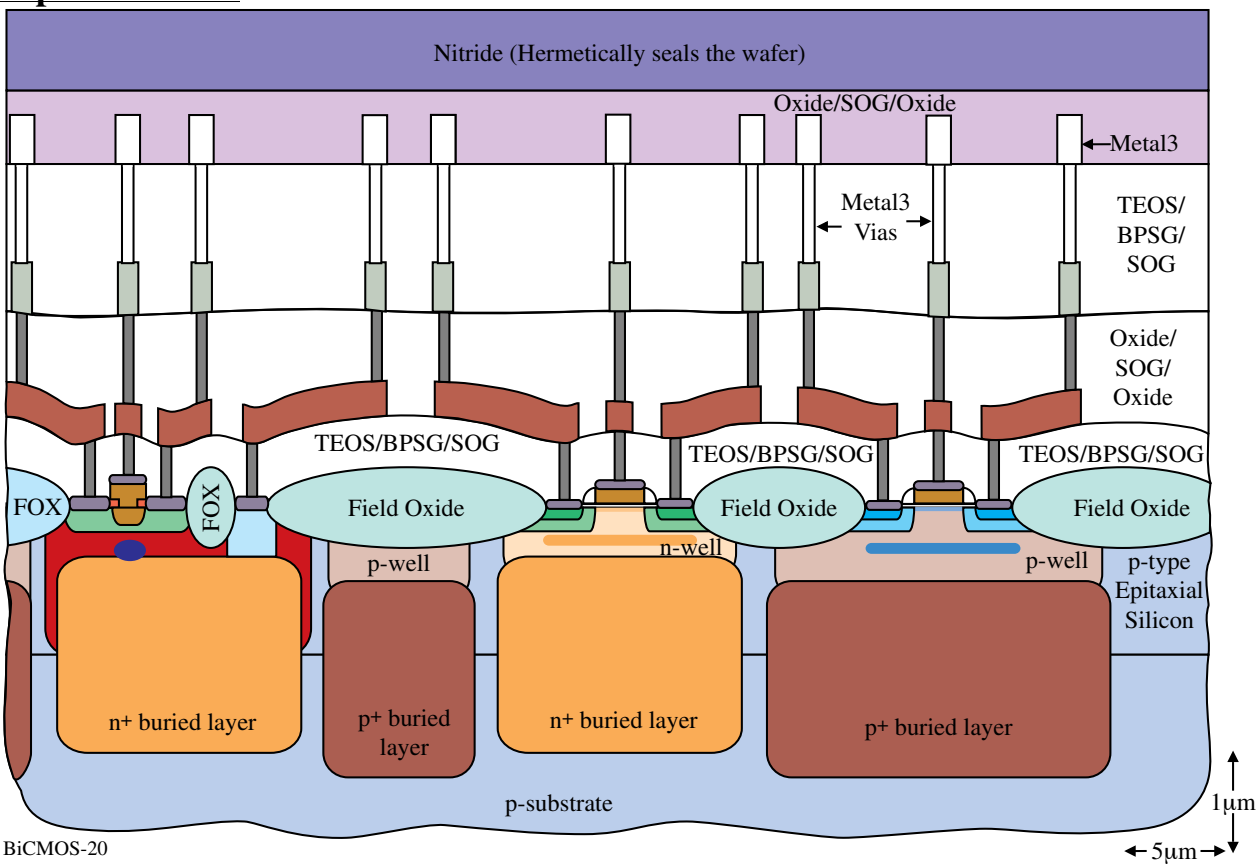


BiCMOS-19

Comments:

- The metal2-metal3 vias will be filled with metal3 as opposed to tungsten plugs

Completed Wafer



BiCMOS-20

SUMMARY

- The basic fabrication steps of a CMOS and BiCMOS technology have been illustrated.
- A modern CMOS technology has f_T's of 20 to 50 GHz and 6 or more levels of metal.
- The active devices of the 0.5micron BiCMOS technology illustrated have the following performance specifications:

  npn bipolar junction transistor:

  f_T = 12GHz, β_F = 100-140 BV_{CEO} = 7V

  n-channel FET:

  K' = 127μA/V^2 V_T = 0.64V $\lambda_N \approx 0.060$

  p-channel FET:

  K' = 34μA/V^2 V_T = -0.63V $\lambda_P \approx 0.072$

- Although today's state of the art is less than 0.5μm BiCMOS, the processing steps illustrated above approximate that which is done in a smaller geometry.
- The next lecture will show how to use these technologies to achieve the all important passive components necessary for the implementation of a frequency synthesizer.