LECTURE 060 – LINEAR PHASE LOCK LOOPS - II

(Reference [2])

LINEAR PHASE LOCKED LOOPS - CONTINUED

THE ACQUISTION PROCESS – LPLL IN THE UNLOCKED STATE

Unlocked Operation

If the PLL is initially unlocked, the phase error, θ_e, can take on arbitrarily large values and as a result, the linear model is no longer valid.

The mathematics behind the unlocked state are beyond the scope of this presentation. In the section we will attempt to answer the following questions from an intuitive viewpoint:

1.) Under what conditions will the LPLL become locked?

2.) How much time does the lock-in process require?

3.) Under what conditions will the LPLL lose lock?

Some Definitions of Key Performance Parameters

1.) The *hold range* ($\Delta\omega_H$) is the frequency range over which an LPLL can statically maintain phase tracking. A PLL is conditionally stable only within this range.

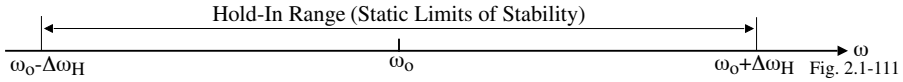


Fig. 2.1-111

2.) The *pull-in range* ($\Delta\omega_P$) is the range within which an LPLL will always become locked, but the process can be rather slow.

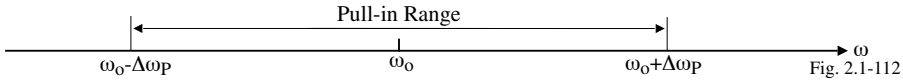


Fig. 2.1-112

3.) The *pull-out range* ($\Delta\omega_{PO}$) is the dynamic limit for stable operation of a PLL. If tracking is lost within this range, an LPLL normally will lock again, but this process can be slow.

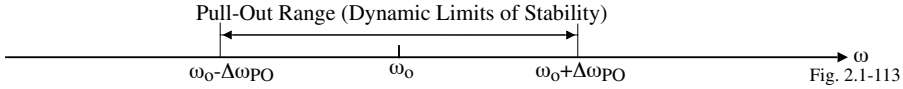


Fig. 2.1-113

4.) The *lock range* ($\Delta\omega_L$) is the frequency range within which a PLL locks within one single-beat note between reference frequency and output frequency. Normally, the operating frequency range of an LPLL is restricted to the lock range.

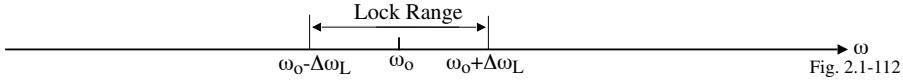


Fig. 2.1-112

Illustration of Static Ranges

Assume the frequency of the VCO is varied very slowly from a value below ω_o-$\Delta\omega_H$ to a frequency above ω_o+$\Delta\omega_H$.

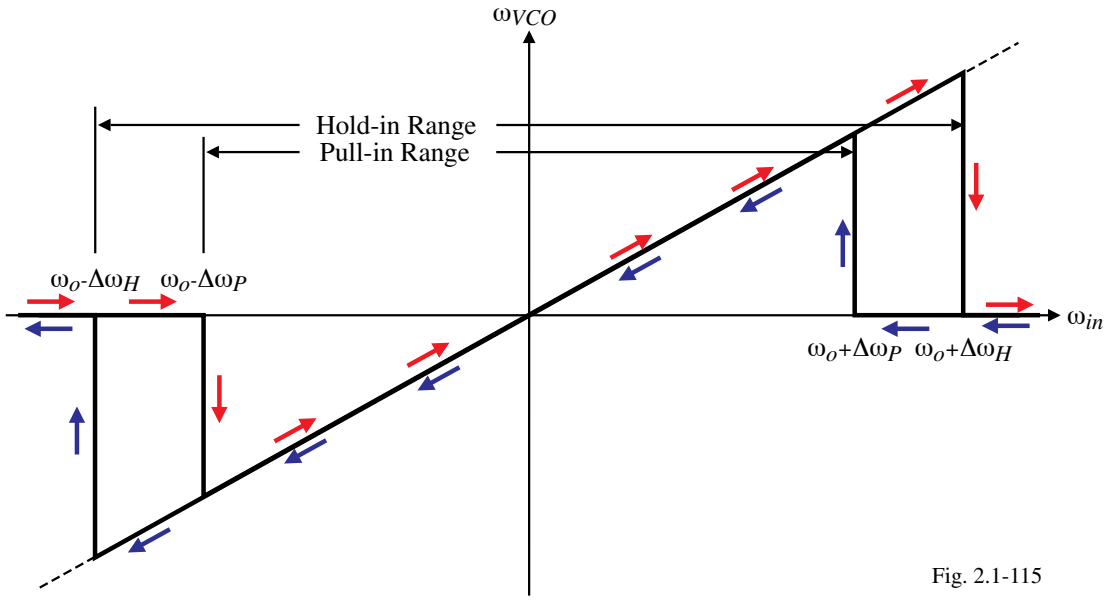


Fig. 2.1-115

The following pages will attempt to relate the key parameters of hold range, pull-in range, pull-out range, and lock range to the time constants, τ_1 and τ_2 and the gain factors K_d, K_o, and K_a.

Hold Range ($\Delta\omega_H$)

The magnitude of the hold range is calculated by finding the frequency offset of the input that causes a phase error of $\pm\pi/2$.

Let,

$$\omega_1 = \omega_o \pm \Delta\omega_H \quad \rightarrow \quad \theta_1(t) = \Delta\omega_H\, t \rightarrow \quad \Theta_1(s) = \frac{\Delta\omega}{s^2}$$

$$\therefore \quad \Theta_e(s) = \Theta_1(s)\, H_e(s) = \frac{\Delta\omega}{s^2}\,\frac{s}{s + K_o K_d F(s)}$$

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} s\Theta_e(s) = \frac{\Delta\omega}{K_o K_d F(0)} \quad \text{(valid for small values of } \theta_e\text{)}$$

For large variations, we write

$$\lim_{t\to\infty} \sin\theta_e(t) = \frac{\Delta\omega_H}{K_o K_d F(0)} \quad \rightarrow \quad \Delta\omega_H = \pm K_o K_d F(0) \text{ when } \theta_e = \pm\pi/2$$

For the various filters-

1.) Passive lag filter: $\Delta\omega_H = \pm K_o K_d$

2.) Active lag filter: $\Delta\omega_H = \pm K_o K_d K_a$

3.) Active PI filter: $\Delta\omega_H = \pm\infty$

(the actual hold range may be limited by the frequency range of the VCO)

Lock Range ($\Delta\omega_L$)

Assume the loop is unlocked and the reference frequency is $\omega_1 = \omega_o + \Delta\omega$. Therefore,

$$v_1(t) = V_{10}\, sin(\omega_o t + \Delta\omega\, t)$$

The VCO output is assumed to be

$$v_2(t) = V_{20}\, sgn(\omega_o t)$$

$$\therefore \quad v_d(t) = K_d\, sin(\Delta\omega\, t) + \text{higher frequency terms}$$

Assuming the higher frequency terms are filtered out, the filter output is

$$v_f(t) \approx K_d |F(j\Delta\omega)|\, sin(\Delta\omega\, t)$$

This signal causes a frequency modulation of the VCO output frequency as shown.

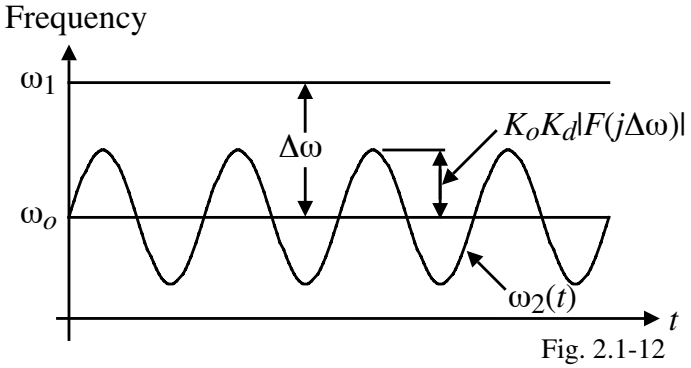


Fig. 2.1-12

Note: No locking occurs in the above illustration because $\Delta\omega > K_o K_d\, |F(j\Delta\omega)|$.

Lock Range – Continued

Locking will take place if $K_o K_d\, |F(j\Delta\omega)| \geq \Delta\omega$. Therefore, the lock range can be expressed as,

$$\Delta\omega_L = \pm\, K_o K_d\, |F(j\Delta\omega)|$$

and is illustrated as,

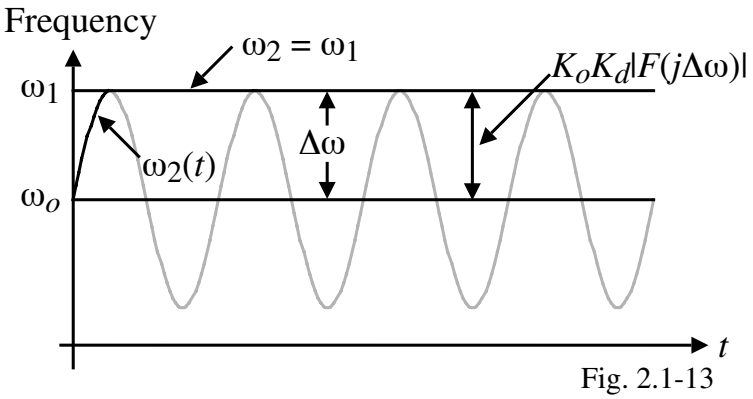


Fig. 2.1-13

Locks within one cycle or beat note.

Lock Range - Continued

If we assume that the lock range is greater than the filter frequencies, $1/\tau_1$ and $1/\tau_2$, the lock range for the various filters can be expressed as,

1.) Passive lag filter: $\Delta\omega_L = \pm K_o K_d \left|F(j\Delta\omega)\right| \approx \pm K_o K_d \dfrac{\tau_2}{\tau_1+\tau_2} \approx \pm K_o K_d \dfrac{\tau_2}{\tau_1}$

2.) Active lag filter: $\Delta\omega_L = \pm K_a \left|F(j\Delta\omega)\right| \approx \pm K_a \dfrac{\tau_2}{\tau_1}$

3.) Active PI filter: $\Delta\omega_L = \pm \left|F(j\Delta\omega)\right| \approx \pm \dfrac{\tau_2}{\tau_1}$

Previously, we found expressions for ω_n and ζ for each type of filter. Using these expressions and assuming that the loop gain is large, we find for all three filters that

$$\Delta\omega_L \approx \pm 2\zeta\omega_n$$

The lock-in time or settling time can be approximated as one cycle of oscillation,

$$T_L \approx \frac{1}{f_n} = \frac{2\pi}{\omega_n}$$

Pull-In Range ($\Delta\omega_P$)

Again assume the loop is unlocked and the reference frequency is $\omega_1 = \omega_o + \Delta\omega$ and the VCO initially operates at the center frequency of ω_o.

Let us re-examine the previous considerations:

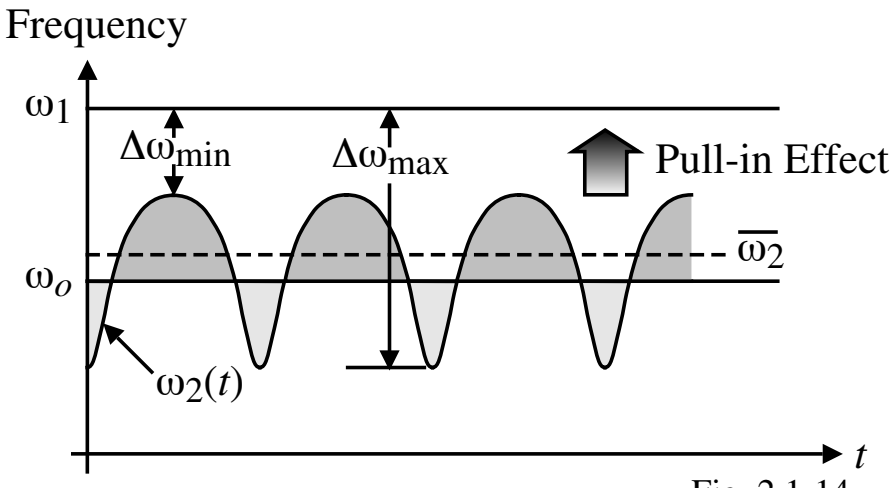


Fig. 2.1-14

Since $\Delta\omega_{\min}$ is less than $\Delta\omega_{\max}$, the frequency of the positive going sinusoid is less than the frequency of the negative going sinusoid. As a consequence, the average value of the VCO output "pulls" toward ω_1.

The Pull-In Process

For an unlocked PLL with the frequency offset, $\Delta\omega$, less than the pull-in range, $\Delta\omega_P$, theVCO output frequency, ω_2 will approach the reference frequency, ω_1, over a time interval called the *pull-in time*, T_P.

Illustration:

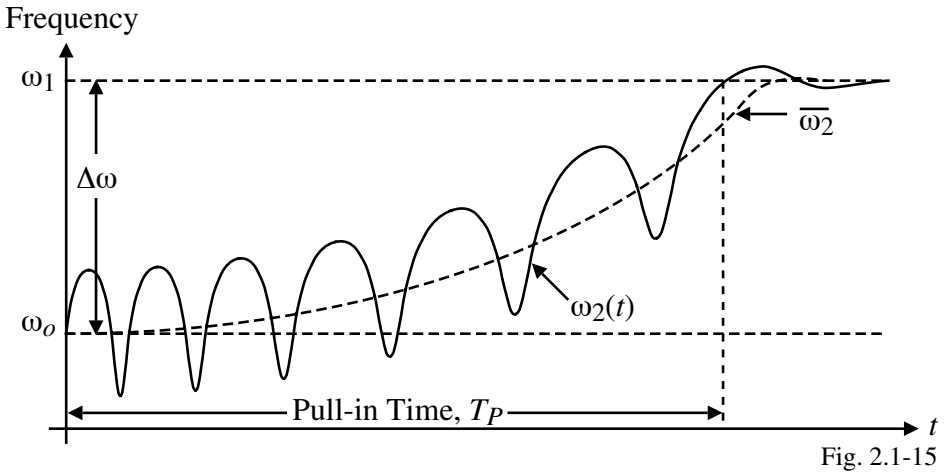


Fig. 2.1-15

Pull-In Range ($\Delta\omega_P$) for Various Types of Filters

The mathematical treatment of the pull-in process is beyond the scope of this presentation[†]. The results are summarized below.

Type of Filter	$\Delta\omega_P$ (Low Loop Gains)	$\Delta\omega_P$ (High Loop Gains)	Pull-In Time, T_P
Passive Lag	$\approx \frac{4}{\pi}\sqrt{2\zeta\omega_n K_o K_d - \omega_n^2}$	$\approx \frac{4\sqrt{2}}{\pi}\sqrt{\zeta\omega_n K_o K_d}$	$= \frac{\pi^2}{16}\frac{\Delta\omega_o^2}{\zeta\omega_n^3}$
Active Lag	$\approx \frac{4}{\pi}\sqrt{2\zeta\omega_n K_o K_d - \frac{\omega_n^2}{K_a}}$	$\approx \frac{4\sqrt{2}}{\pi}\sqrt{\zeta\omega_n K_o K_d}$	$= \frac{\pi^2}{16}\frac{\Delta\omega_o^2 K_a}{\zeta\omega_n^3}$
Active PI Lag	$\rightarrow \infty$	$\rightarrow \infty$	$= \frac{\pi^2}{16}\frac{\Delta\omega_o^2}{\zeta\omega_n^3}$

[†] R.M. Best, *Phase-Locked Loops – Design, Simulation, and Applications*, 4th ed., McGraw-Hill Book Co., 1999, Appendix A.

Example

A second-order PLL having a passive lag loop filter is assumed to operate at a center frequency, f_o, of 100kHz and has a natural frequency, f_n, of 3 Hz which is a very narrow band system. If $\zeta = 0.7$ and the loop gain, $K_o K_d = 2\pi \cdot 1000$ sec.$^{-1}$, find the lock-in time, T_L, and the pull-in time, T_P, for an initial frequency offset of 30 Hz.

Solution

$$T_L \approx \frac{1}{f_n} = \frac{1}{3} = 0.333 \text{ secs.}$$

$$T_P = \frac{\pi^2}{16}\frac{\Delta\omega_o{}^2}{\zeta\omega_n{}^3} = \frac{4\pi^4}{16 \cdot 8\pi^3}\frac{\Delta f_o{}^2}{\zeta f_n{}^3} = \frac{\pi\, 30^2}{32(0.7)3^3} = 4.675 \text{ secs.}$$

Pull-Out Range ($\Delta\omega_{PO}$)

The pull-out range is that *frequency step* which causes a lock-out if applied to the reference input of the PLL.

An exact calculation is not possible but simulations show that,

$$\Delta\omega_{PO} = 1.8\omega_n\,(\zeta + 1)$$

At any rate, the pull-out range for most systems is between the pull-in range and the lock-range,

$$\Delta\omega_L < \Delta\omega_{PO} < \Delta\omega_P$$

Steady-State Error of the PLL

The steady-state error is the deviation of the controlled variable from the set point after the transient response has died out. We have called this error, $\theta_e(\infty)$.

$$\theta_e(\infty) = \lim_{s\to 0} s\Theta_e(s) = \lim_{s\to 0} s\Theta_1(s)\frac{s}{s + K_o K_d F(s)}$$

Let us consider a generalized filter given as,

$$F(s) = \frac{P(s)}{Q(s)s^N}$$

where $P(s)$ and $Q(s)$ can be any polynomials in s, and N is the number of poles at $s = 0$.

$$\therefore \qquad \theta_e(\infty) = \lim_{s\to 0} \frac{s^2 s^N Q(s)\Theta_1(s)}{s\cdot s^N Q(s) + K_o K_d P(s)}$$

Comments:

- Note that for the active PI filter, $N = 1$.
- For $N > 1$, it becomes difficult to maintain stability.
- In most cases, $P(s)$ is a first-order polynomial and $Q(s)$ is a polynomial of order 0 or 1.

To find the steady-state error, the input, $\Theta(s)$ must be known. We will consider several inputs on the following slide.

Steady-State Error for Various Inputs

1.) A phase step, $\Delta\Phi$.

$$\Theta_1(s) = \frac{\Delta\Phi}{s}$$

$$\therefore \qquad \theta_e(\infty) = \lim_{s\to 0} \frac{s^2 s^N Q(s)\Delta\Phi}{s[s\cdot s^N Q(s) + K_o K_d P(s)]} = 0 \text{ for any value of } N.$$

2.) A frequency step, $\Delta\omega$.

$$\Theta_1(s) = \frac{\Delta\omega}{s^2}$$

$$\therefore \qquad \theta_e(\infty) = \lim_{s\to 0} \frac{s^2 s^N Q(s)\Delta\omega}{s^2[s\cdot s^N Q(s) + K_o K_d P(s)]} = 0 \text{ if } N \geq 1$$

(The LPLL must have one pole at $s = 0$ for the steady-state error to be zero.)

3.) A frequency ramp, $\Delta\dot{\omega}$.

$$\Theta_1(s) = \frac{\Delta\dot{\omega}}{s^3}$$

$$\therefore \qquad \theta_e(\infty) = \lim_{s\to 0} \frac{s^2 s^N Q(s)\Delta\dot{\omega}}{s^3[s\cdot s^N Q(s) + K_o K_d P(s)]} = 0 \text{ if } N \geq 2$$

For $N = 2$ and $Q(s) = 1$, the order of the LPLL becomes 3 permitting a phase shift of nearly 270° which must be compensated for by zeros to maintain stability.

NOISE IN LINEAR PLL SYSTEMS

Phase Noise

Illustration:

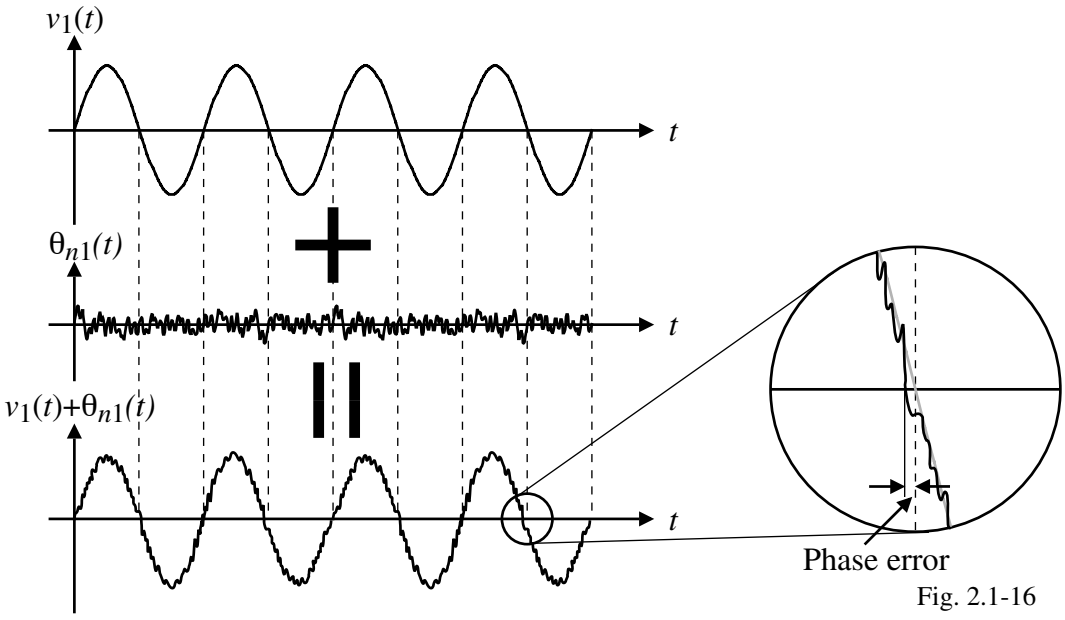


Fig. 2.1-16

PLL for Noise Analysis

Assume that the input is band limited as shown below.

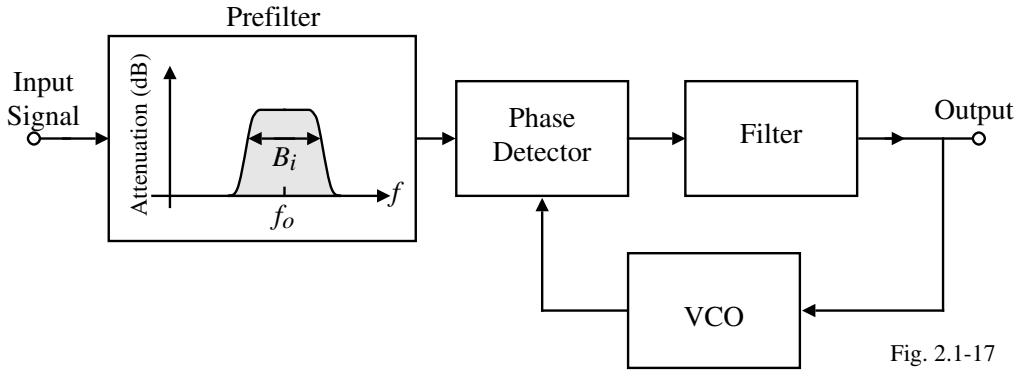


Fig. 2.1-17

B_i = Bandwidth of the prefilter (or system)

Some terminology:

- Power spectral density is the measure of power in a given frequency range (Watts/Hz) or (V^2/Hz). It is found by dividing the rms power by the bandwidth.
- We will consider all noise signals as white noise which means the power spectrum is flat.
- P_s = input signal rms power ($V_1(\text{rms})^2/R_{in}$)
- P_n = rms power of the input noise

Power Spectra of a PLL

Illustration of how input noise becomes phase noise in the frequency spectrum:

Power spectra of the reference signal, $v_1(t)$, and the superimposed noise signal, $v_n(t)$.

Spectrum of the phase noise at the input of the PLL.

Frequency response of the phase-transfer function, $H(j\omega)$.

Spectrum of the phase noise at the output of the PLL.

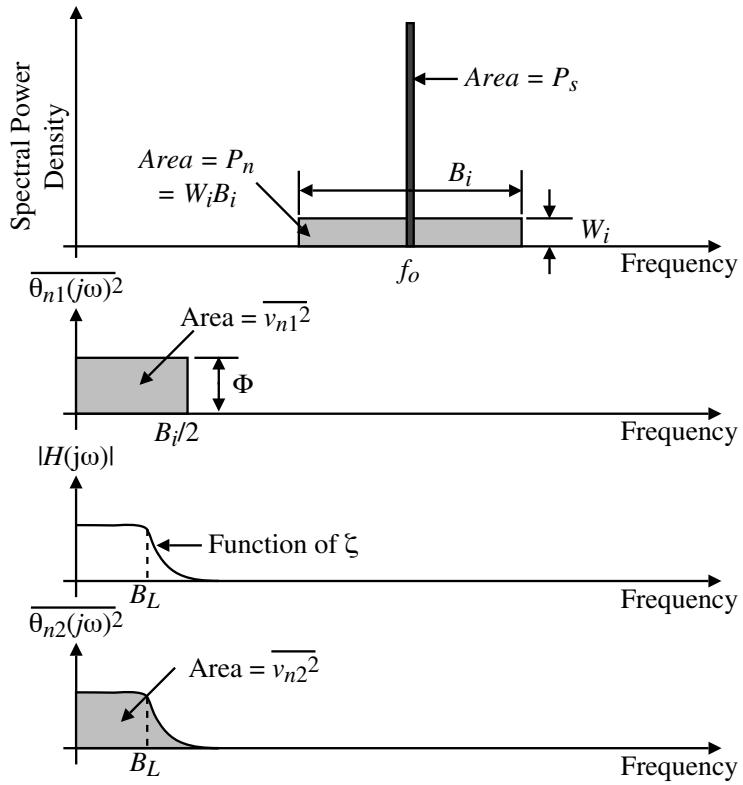


Fig. 2.1-18

Noise Relationships for a PLL

Spectral density of the input noise signal:

$$W_i = \frac{P_n}{B_i} \text{ (W/Hz)}$$

Input rms phase noise jitter (or the square of the rms phase noise):

$$\theta_{n1}(t) \rightarrow \overline{\theta_{n1}^2} = \frac{P_n}{2P_s}$$ (Comes from the assumption of white noise)

Signal-to-Noise Ratio (SNR):

$$SNR \text{ at the input} = (SNR)_i \equiv \frac{P_s}{P_n} \rightarrow \overline{\theta_{n1}^2} = \frac{P_n}{2P_s} = \frac{1}{2(SNR)_i} \text{ (radians}^2\text{)}$$

Input phase jitter (noise) spectrum:

$$\overline{\Theta_{n1}^2(j\omega)} = \Phi = \frac{\overline{\theta_{n1}^2}}{B_i/2} \text{ (radians}^2\text{/Hz)}$$

Output phase jitter (noise) spectrum:

$$\overline{\Theta_{n2}^2(j\omega)} = |H(j\omega)|^2 \overline{\Theta_{n1}^2(j\omega)} = |H(j\omega)|^2 \Phi$$

RMS Value of the Output Phase Noise

The output phase noise is found by integrating $\Theta_{n2}(j\omega)$ over the bandwidth of the PLL.

$$\overline{\theta_{n2}^2} = \int_0^\infty \overline{\Theta_{n2}^2(j2\pi f)}\, df$$

where $\overline{\theta_{n2}^2}$ is the area under the output phase noise plot in a previous slide.

$$\overline{\theta_{n2}^2} = \int_0^\infty |H(j\omega)|^2 \Phi df = \frac{\Phi}{2\pi}\int_0^\infty |H(j\omega)|^2 d\omega$$

What is the value of $\int_0^\infty |H(j\omega)|^2 d\omega$?

Let $\int_0^\infty |H(j2\pi f)|^2 df = B_L$ = the noise bandwidth.

The solution of this integral is,

$$B_L = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right) \rightarrow \frac{dB_L}{d\zeta} = \frac{\omega_n}{2}\left(1 - \frac{1}{2\zeta}\right) = 0 \rightarrow \zeta = 0.5 \rightarrow B_L(\min) = 0.5\omega_n$$

$$\therefore \quad \overline{\theta_{n2}^2} = \Phi B_L = \frac{\overline{\theta_{n1}^2}}{B_i/2} B_L = \frac{P_n}{2P_s}\frac{2B_L}{B_i} = \frac{P_n}{P_s}\cdot\frac{B_L}{B_i} = \frac{B_L}{(SNR)_i B_i}$$

RMS Value of the Output Phase Noise – Continued

We noted previously that,

$$\overline{\theta_{n1}^2} = \frac{1}{2(SNR)_i}$$

A dual relationship holds for the output,

$$\overline{\theta_{n2}^2} = \frac{1}{2(SNR)_L}$$

where $(SNR)_L$ is the signal-to-noise ratio at the output.

$$\therefore \quad (SNR)_L = (SNR)_i \frac{B_i}{2B_L}$$

This equation suggests that the PLL improves the *SNR* of the input signal by a factor of $B_i/2B_L$. Thus, the narrower the noise PLL bandwidth, B_L, the greater the improvement.

Some experimental observations:

- For $(SNR)_L = 1$, a lock-in process will not occur because the output phase noise is excessive.
- At an $(SNR)_L = 2$, lock-in is eventually possible.
- For $(SNR)_L = 4$, stable operation is generally possible.

Note: $(SNR)_L = 4$, $\overline{\theta_{n2}^2}$ becomes 0.125 radians^2. $\sqrt{\theta_{n2}^2} = 0.353$ radians $\Rightarrow 20°$ and the limit of dynamic stability (180°) is rarely exceeded.

Summary of Noise Analysis of the LPLL

- Stable operation of the LPLL is possible if $(SNR)_L \geq 4$
- $(SNR)_L$ is calculated from

$$(SNR)_L = \frac{P_s}{P_n}\frac{B_i}{2B_L}$$

where P_s = signal power at the reference input

P_n = noise power at the reference point

B_i = bandwidth of the system at the input

B_L = noise bandwidth of the PLL

- The noise bandwidth, B_L, is a function of ω_n and ζ. For $\zeta = 0.7$, $B_L = 0.53\omega_n$
- The average time interval between two unlocking events gets longer as the $(SNR)_L$ increases.

Pull-In Techniques for Noisy Signals

1.) The sweep technique.

When the noise bandwidth is made small, the *SNR* of the loop is sufficiently large to provide stable operation. However, the lock range can become smaller than the frequency interval $\Delta\omega$ within which the input signal is expected to be. The following circuit solves this problem by providing a direct VCO sweep.

(1.) LPLL not locked.

(2.) RUN mode starts a positive sweep.

(3.) When the VCO frequency approaches the input frequency the loop locks.

(4.) The "In-Lock" detector switches the sweep switch to the "HOLD" position.

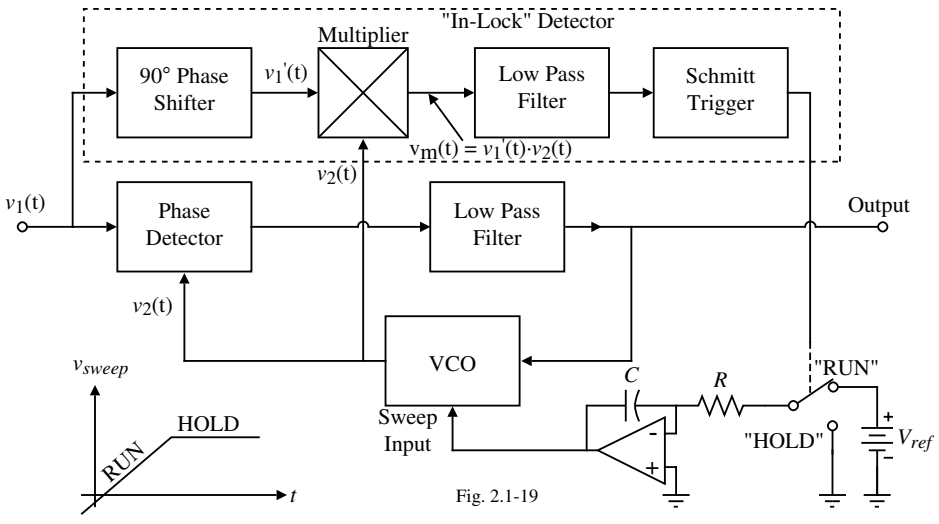


Fig. 2.1-19

Pull-In Techniques for Noisy Signals

2.) Switched filter technique.

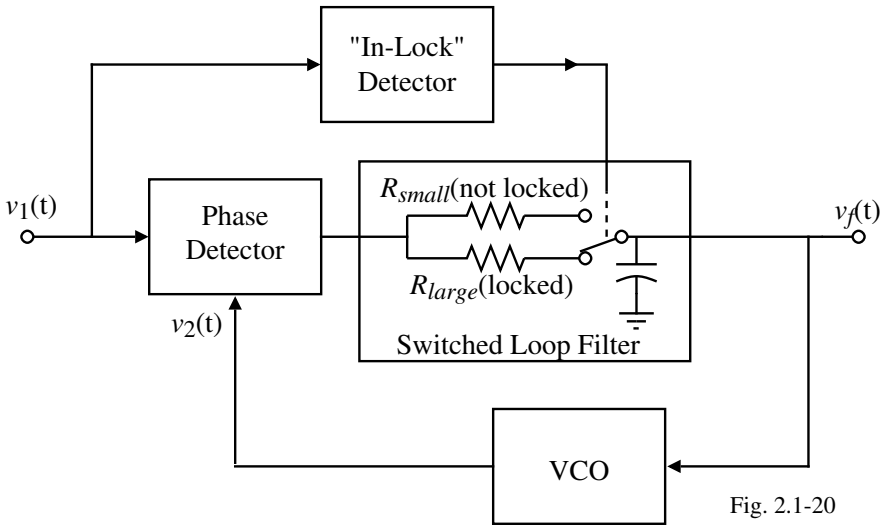


Fig. 2.1-20

In the unlocked state, the filter bandwidth is large so that lock range exceeds the frequency range within which the input is expected.

In the locked state, the filter bandwidth is reduced in order to reduce the noise.

LPLL SYSTEM DESIGN

Design Procedure

Objective: Design the parameters K_o, K_d, ζ, and the filter $F(s)$ of the LPLL.

Given: The phase detector and VCO and pertinent information concerning these blocks.

Steps:

1.) Specify the center frequency, ω_o, and its range $\omega_{o\min}$ and $\omega_{o\max}$.

2.) Select the value of ζ. Small values give an overshoot and large values are slow. $\zeta = 0.7$ is typically a good value to choose.

3.) Specify the lock range $\Delta\omega_L$.

a.) If noise can be neglected, then the selected value of $\Delta\omega_L$ is chosen.

b.) If noise cannot be neglected, then use the input noise SNR, $(SNR)_i$ and the input noise bandwidth, B_i, to find the noise bandwidth, B_L. Later when we find ω_n, the value of $\Delta\omega_L$ will be specified.

4.) Specify the frequency range of the LPLL as $\omega_{2\min}$ and $\omega_{2\max}$ as,

$\omega_{2\min} < \omega_{o\min} - \Delta\omega_L$ and $\omega_{2\max} > \omega_{o\max} + \Delta\omega_L$

Some practical limits are,

$\omega_{2\min} = \omega_{o\min} - 1.5\Delta\omega_L$ and $\omega_{2\max} = \omega_{o\max} + 1.5\Delta\omega_L$

Design Procedure – Continued

5.) Design of the VCO. From the power supply voltage or data sheet find the value of K_o as shown below.

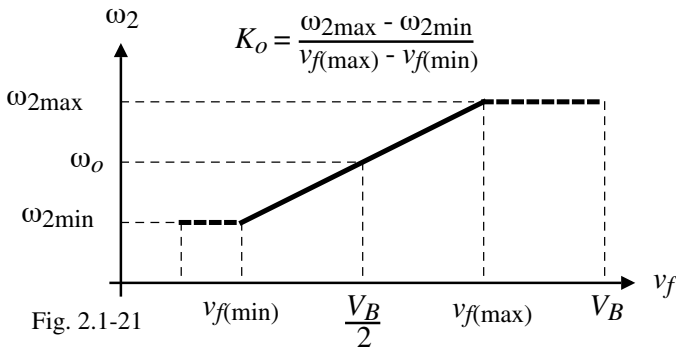


Fig. 2.1-21

6.) Determine the value of K_d from the data sheet. K_d will depend upon the signal level. It is preferred to have a large value of K_d.

7.) Determine the natural frequency, ω_n.

a.) Lock range has been specified in step 3.).

$$\omega_n = \frac{\Delta\omega_L}{2\zeta}$$

b.) Noise bandwidth has been specified in step 3.)

$$\omega_n = \frac{2B_L}{\zeta + 0.25\zeta}$$

Design Procedure – Continued

8.) Select the type of loop filter.

a.) Passive lag filter:

Solve for τ_1 and τ_2 from the following equations. Normally, τ_1 should be 5-10 times τ_2. If this is not the case, choose another type of filter.

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau_1 + \tau_2}} \qquad \text{and} \qquad \zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K_o K_d}\right)$$

b.) Active lag filter:

Use the following equations to solve for τ_1, τ_2, and K_a. It will be necessary to choose one of these parameters because there are only two equations.

$$\omega_n = \sqrt{\frac{K_o K_d K_a}{\tau_1}} \qquad \text{and} \qquad \zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K_o K_d K_a}\right)$$

c.) Active PI filter:

Use the following equations to solve for τ_1 and τ_2. Because this filter has a pole at $s = 0$, it is not necessary for τ_1 to be larger than τ_2.

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau_1}} \qquad \text{and} \qquad \zeta = \frac{\omega_n \tau_2}{2}$$

LPLL Design Example

Consider the multichannel telemetry system shown where one single, voice-grade communication line is used to transmit a number of signal channels.

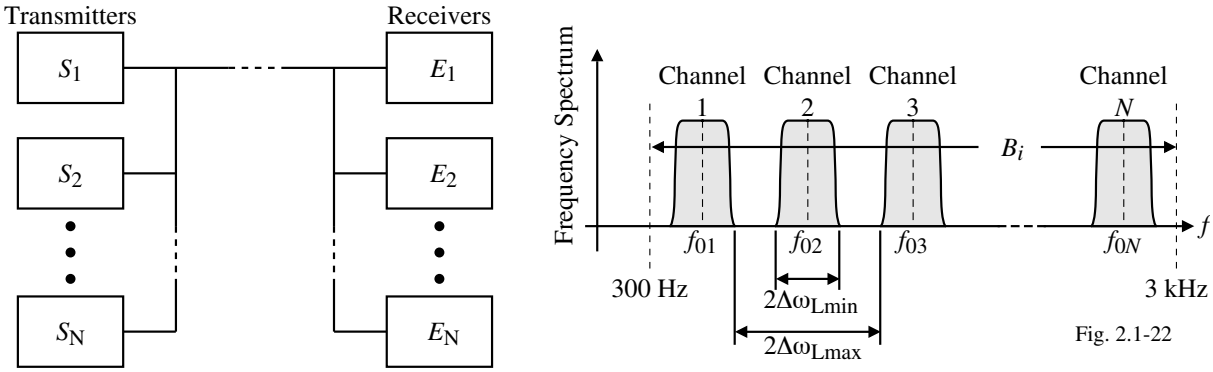


Fig. 2.1-22

Each transmitter is to transmit a binary signal with a baud rate of 50 bits/sec. The signal is encoded in a non-return to zero format which means that the bandwidth required is half the baud rate or 25 Hz. The spectrum of the FM-modulated carrier consists of the carrier frequency and a number of sidebands displaced by ±25 Hz, ±2·25 Hz, etc. from the carrier frequency.

Assuming that a narrow-band FM is used, the channel spacing will be selected as 60 Hz. The channel is assumed to be an ordinary telephone cable with a bandwidth of 300 Hz to 3000 Hz giving B_i = 2700 Hz. Therefore, the maximum number of channels is

Max. no. of channels = B_i/Channel spacing = 2700/60 = 45 channels.

LPLL Design Example – Continued

Design one of the receivers using the procedure outlined above assuming the carrier frequency is 1000 Hz. Assume the VCO is an XR-215[†]

1.) The angular frequency, ω_o, is $2\pi\cdot 1000 = 6280$ sec.$^{-1}$.

2.) Select $\zeta = 0.7$.

3.) In this problem the noise cannot be neglected. Therefore, we must find the noise bandwidth, B_L, of the loop and not the lock-range $\Delta\omega_L$. The input *SNR* is given as

$$(SNR)_i = \frac{P_s}{P_n}$$

Because there are 44 other channels, let the noise of our particular channel be $P_n = 44P_s$. Therefore,

$$(SNR)_i = \frac{P_s}{P_n} = \frac{1}{44} \approx 0.023$$

To enable locking onto the carrier, the *SNR* of the loop should be approximately 4.

$$\therefore \qquad B_L = \frac{(SNR)_i B_i}{(SNR)_L 2} = \frac{0.023\cdot 2700}{4\cdot 2} = 7.67 \text{ Hz}$$

4.) Determine the lock range. Because the noise bandwidth, B_L, is very small, the lock range will be small and will be determined in step 7.

[†] *Phase-Locked Loop Data Book*, Exar Integrated Systems, Sunnyvale, CA, 1981.(http://www.exar.com/products/XR215A.html)

LPLL Design Example – Continued

5.) From the data sheet of the VCO we get,

$$f_o = \frac{200}{C_o}\left(1 + \frac{0.6}{R_x}\right) \text{ and } K_o = \frac{700}{C_o R_o}$$

where the resistors are in kΩ and the capacitors in μF.

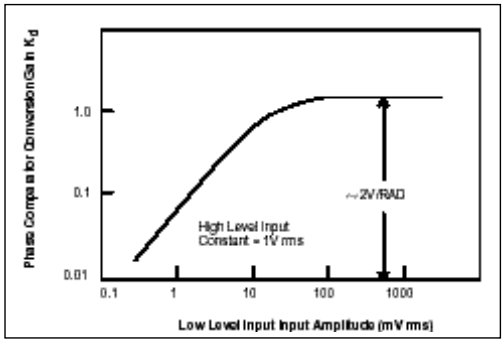
Choosing $C_o = 0.27\mu F$ and $R_x = 1.71k\Omega$ gives the required center frequency of 1000 Hz.

The data sheet specifices that R_o should be in the range of 1 to 10 kΩ. Therefore, we see that K_o can be in the range of 260 rads/sec·V to 2600 rads/sec·V. Choosing R_o as 10 kΩ, gives $K_o = 260$ rads/sec·V.

This means that the VCO can change its frequency by $260/2\pi = 41.4$ Hz. We will have to check in step 7 that this range is sufficient to enable locking within the lock range of $\Delta\omega_L$.

6.) Determine K_d. A plot of the data sheet is shown. In the application we are considering, the input signal level is 3mV(rms).

$\therefore\ K_d \approx 0.2$ V/rad/



LPLL Design Example – Continued

7.) ω_n is calculated from B_L and ζ and is,

$$\omega_n = \frac{2B_L}{\zeta + 0.25\zeta} = \frac{2\cdot 7.67}{0.7\cdot 1.25} = 17.53 \text{ sec.}^{-1}$$

The lock-in range is found as,

$$\Delta\omega_L = 2\zeta\omega_n = 24.54 \text{ sec.}^{-1}$$

8.) Solve for τ_1 and τ_2 from the equations below.

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau_1+\tau_2}} \qquad \text{and} \qquad \zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K_o K_d}\right)$$

$$\tau_2 = \frac{2\zeta}{\omega_n} - \frac{1}{K_o K_d} = 60.6 \text{ ms}$$

$$\tau_1 + \tau_2 = \frac{K_o K_d}{\omega_n^2} = 169.2 \text{ ms} \rightarrow \quad \tau_1 = 108.6 \text{ ms}$$

The resistor R_1 is already integrated on the chip as 6 kΩ.

9.) Finally, determine R_1, R_2, and C of the filter. The data sheet shows that the resistor, R_1, is already integrated on the chip as 6 kΩ. (Note: Two passive lag filters are needed.)

$$\therefore \quad C = \frac{\tau_1}{R_1} = \frac{108.6 \text{ ms}}{6 \text{ k}\Omega} = 18.1 \ \mu\text{F} \qquad \text{and} \qquad R_2 = \frac{\tau_2}{C} = \frac{60.6 \text{ ms}}{18.1 \ \mu\text{F}} = 3.35 \text{ k}\Omega$$

Simulation of the LPLL Design Example

The open loop transfer function is,

$$LG(s) = \frac{K_v}{s}\left(\frac{1+s\tau_1}{1+s(\tau_1+\tau_2)}\right) = \frac{52}{s}\left(\frac{1+s60.6\text{x}10^{-3}}{1+s169.2\text{x}10^{-3}}\right)$$

Cutoff frequency:

$$\omega_c = \omega_n\sqrt{2\xi^2+\sqrt{4\xi^4+1}} = 17.53\sqrt{2\cdot 0.7^2+\sqrt{4\cdot 0.7^4+1}} = 27.045 \text{ rads/sec} \quad (4.3 \text{ Hz})$$

The phase margin can be written as,

$$PM = 180° - 90° + \tan^{-1}(\omega_c\cdot 60.6\text{x}10^{-3}) - \tan^{-1}(\omega_c\cdot 169.2\text{x}10^{-3})$$

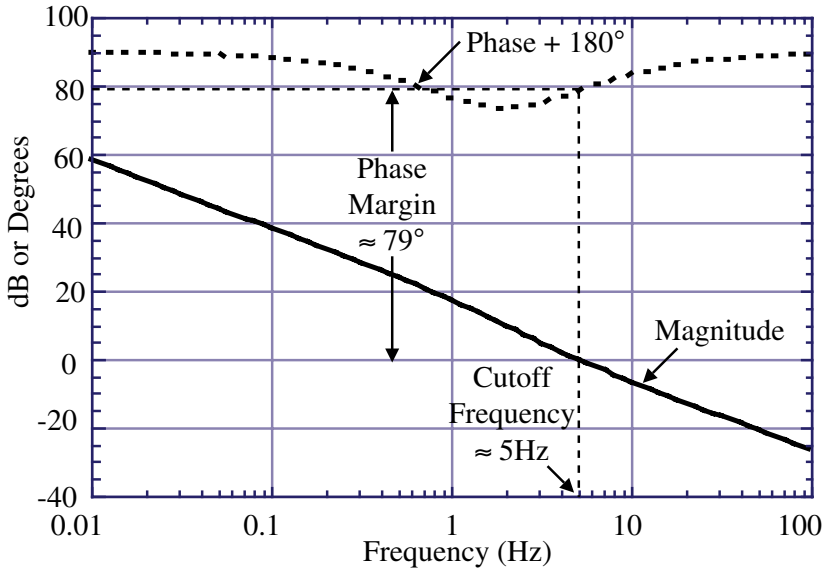
$$= 90° + 58.61° - 77.67° = 70.94°$$

PSPICE Input File:

```
LPLL Design Problem-Open Loop Response
VS 1 0 AC 1.0
R1 1 0 10K
* Loop bandwidth = Kv =52 sec.-1   Tau1=60.6E-3  Tau2=108.6E-3
ELPLL 2 0 LAPLACE {V(1)}= {(52/(S+0.00001))*((1+60.6E-3*S)/(1+108.6E-3*S))}
R2 2 0 10K
*Steady state AC analysis
.AC DEC 20 0.01 100
.PRINT AC VDB(2) VP(2)
.PROBE
.END
```


Simulation of the LPLL Design Example - Continued

Open Loop Response

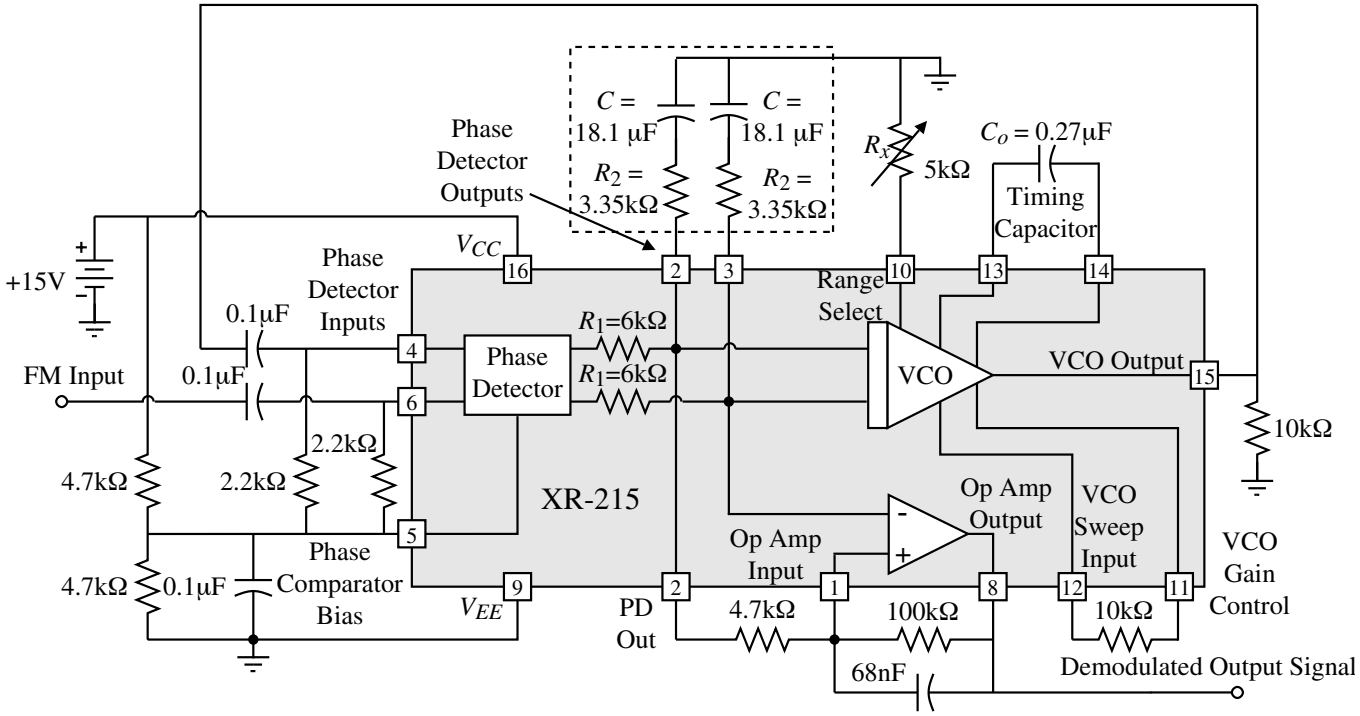


Cutoff frequency ≈ 5Hz

Phase margin ≈ 79°

LPLL Design Example – Continued

Implementation of the FSK Demodulator:



LPLL SYSTEM SIMULATION

A PC-based simulation program developed by R.M. Best and found as part of the 4th edition is used as an example of PLL simulation at the systems level. The description of how to use this program is found on the CD or described in the text, *Phase-Locked Loops-Design, Simulation, and Applications*, 4th ed., 1999, McGraw-Hill Book Co.

The simulation flow chart is show below and follows the previous design procedure.

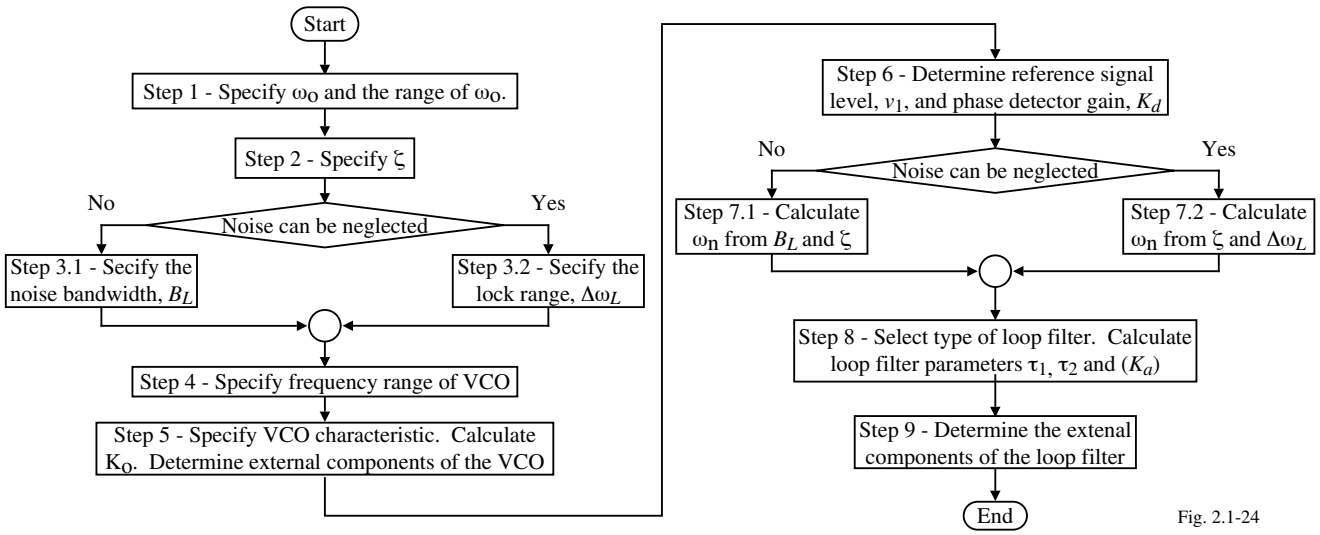


Fig. 2.1-24

Example of LPPL Simulation

PLL selected is:

1.) Architecture - LPLL, Passive Lag, and VCO

2.) Parameters –

Power supply = +5V and 0V

Phase detector: $K_d = 1.0$, $V_{sat}^+ = 4.5$V and $V_{sat}^- = 0.5$V

Loop filter: $\tau_1 = 500$ µsec. and $\tau_2 = 50$ µsec.

Oscillator: $K_o = 130{,}000$ rads/sec·V, $V_{sat}^+ = 4.5$V and $V_{sat}^- = 0.5$V

The simulator program calculates $\omega_n = 15{,}374.12$ rads/sec. and $\zeta = 0.443$.

Using the formulas developed in these notes, we can compute the key LPLL parameters as:

1.) Lock range: $\Delta\omega_L = 13{,}621$ rads/sec. $\rightarrow$ $\Delta f_L = 2169$ Hz

2.) Pull-out range: $\Delta\omega_{PO} = 39{,}932$ rads/sec. $\rightarrow$ $\Delta f_{PO} = 6358$ Hz

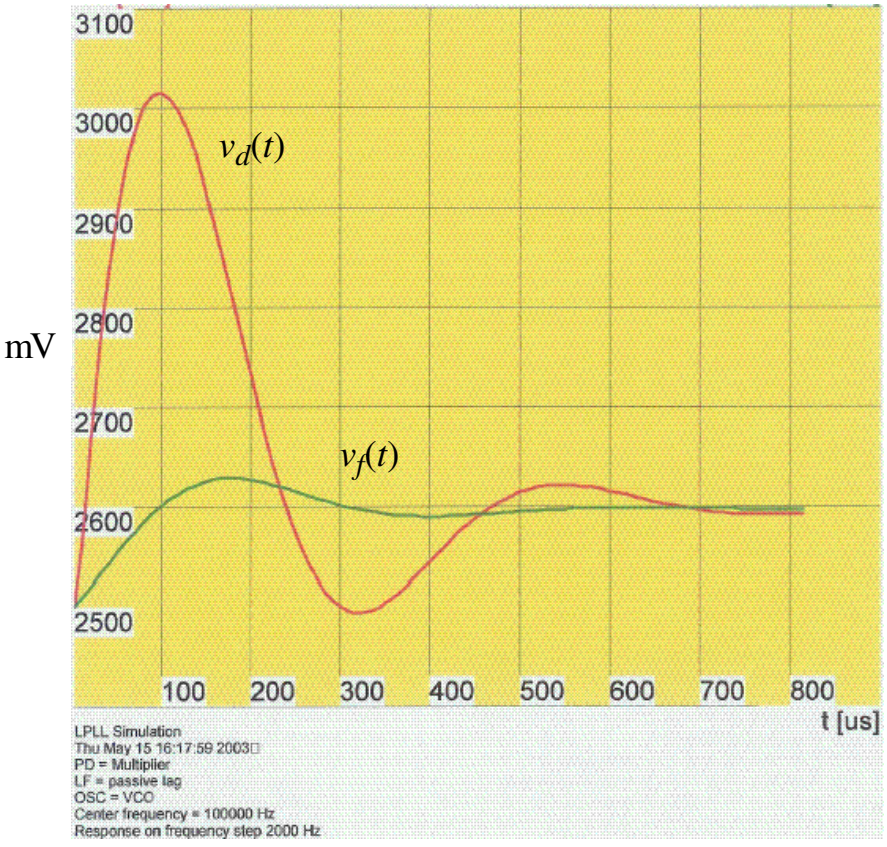
3.) Pull-in range: $\Delta\omega_P = 53{,}597$ rads/sec. $\rightarrow$ $\Delta f_P = 8534$ Hz

(The ratio $\frac{\omega_n}{K_o K_d} = 0.12$ and can be considered a high-gain loop)

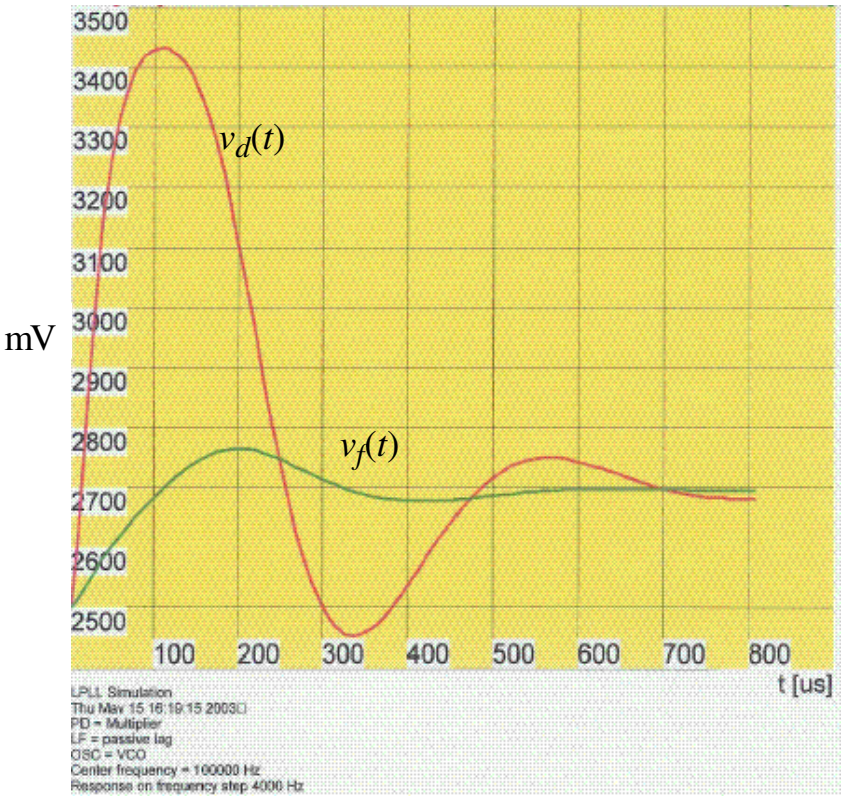
4.) Hold range: $\Delta\omega_H = 130{,}000$ rads/sec. $\rightarrow$ $\Delta f_L = 20{,}700$ Hz

On the following pages, we attempt to verify these values by simulation.

Pull-out Range of the LPLL (2kHz Frequency Step)



Linearity of the LPLL (Frequency Step Doubled from 2kHz to 4kHz)

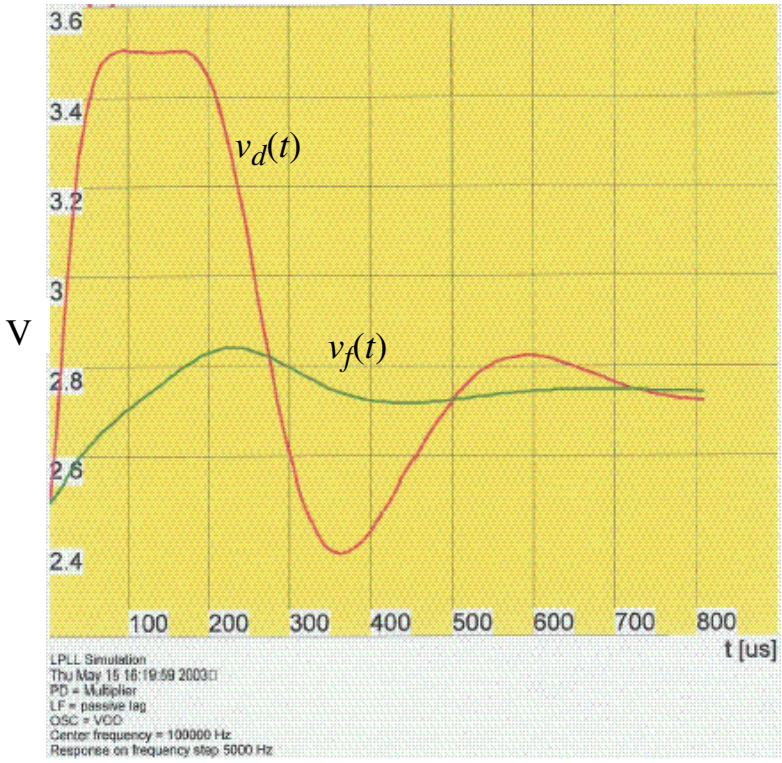


The LPLL is not linear because doubling the frequency step did not double the output.

The flat topped response for $v_d(t)$ indicates that the phase error is close to $\pi/2$.

Loop is still locked.

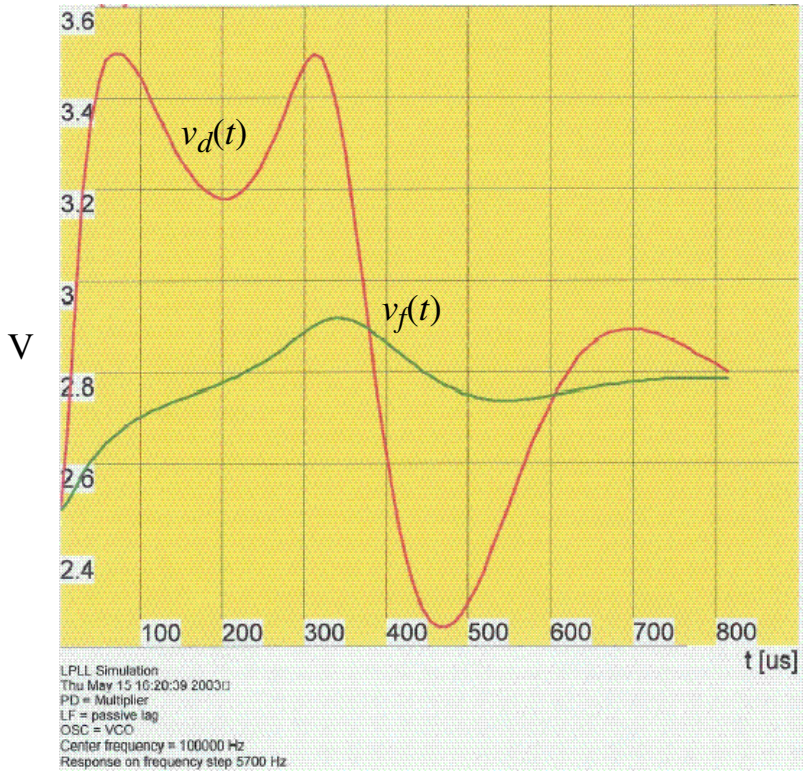
Pull-out Range of the LPLL (Frequency = 5kHz)



The dip in the response of the detector output implies that the phase error has exceeded $\pi/2$.

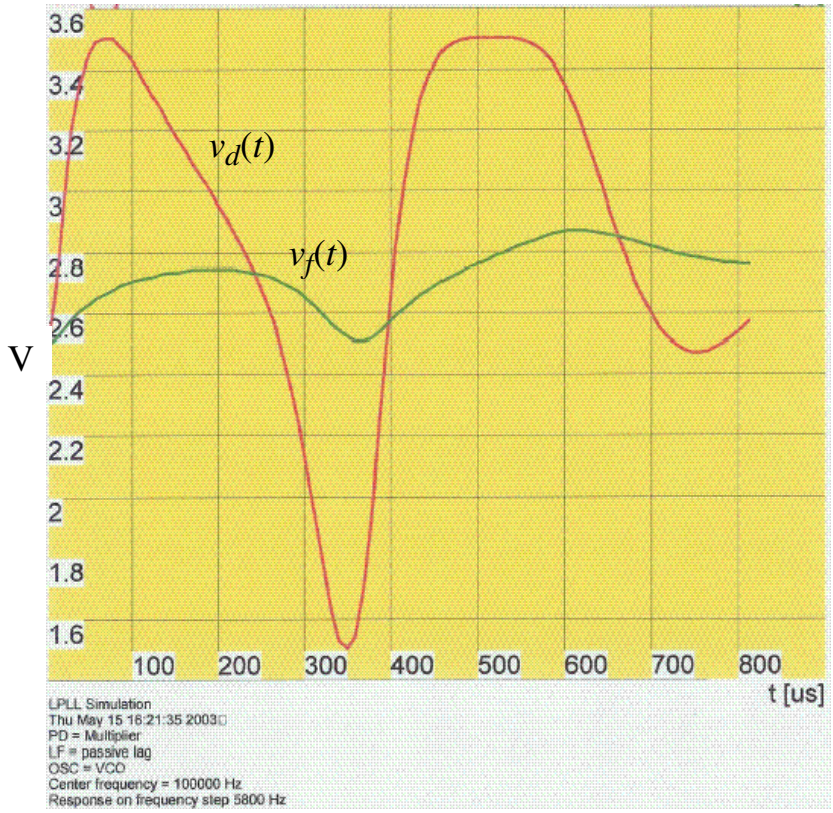
The loop is still locked.

Finding the Pull-out Range (Frequency step = 5700Hz)



The loop has not yet pulled out and is still locked.

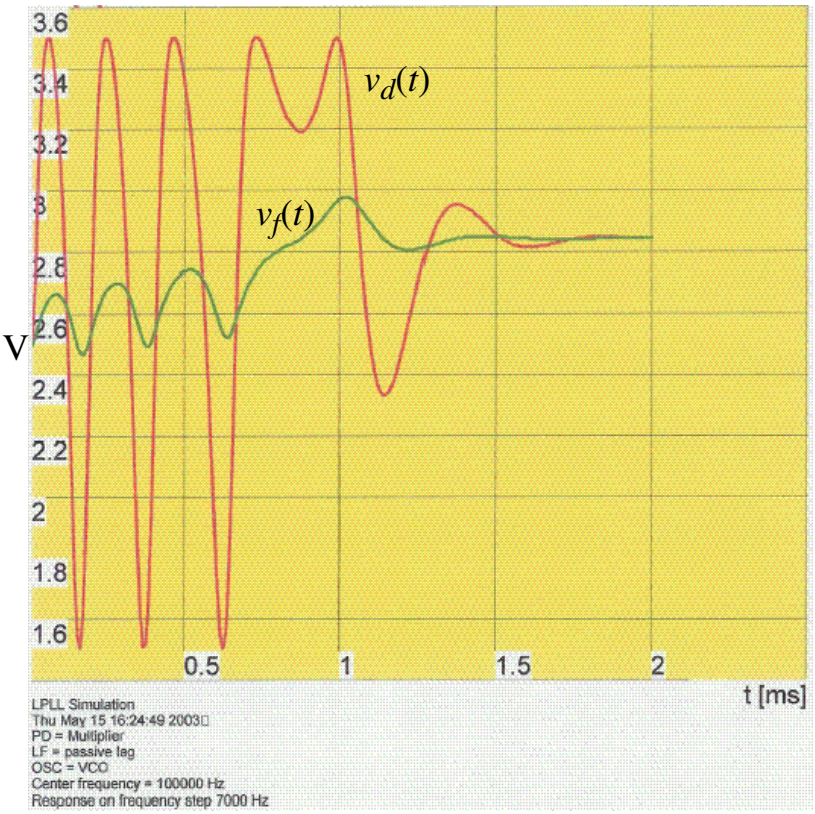
Finding the Pull-out Frequency (Frequency step = 5800Hz)



From this simulation, we see that the pull-out frequency is close to 5800Hz which is compared with the predicted value of 6358Hz (10% error).

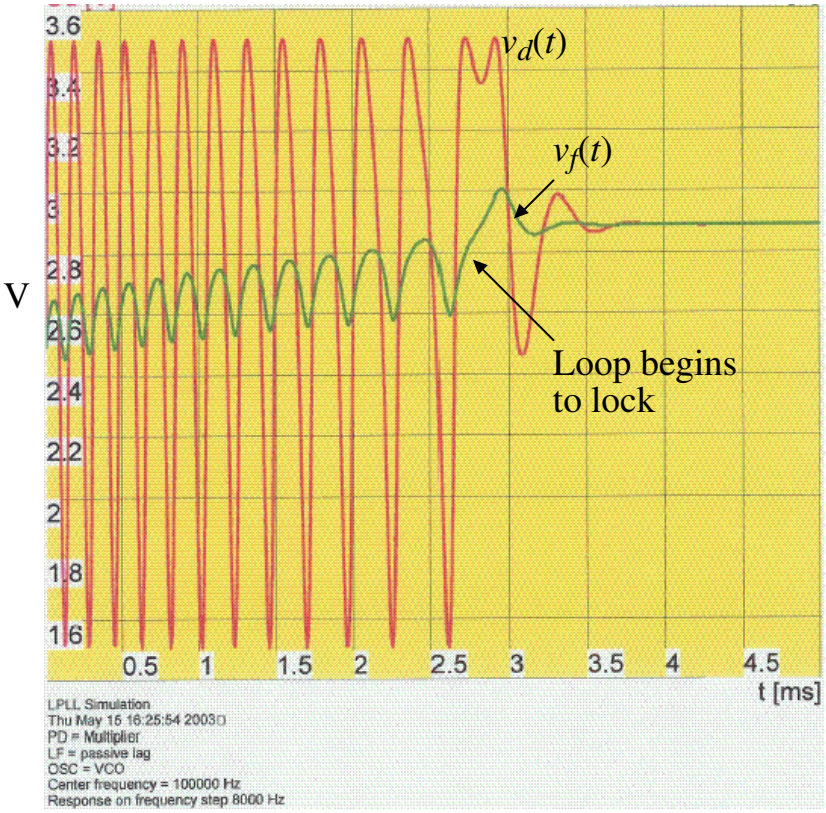
Because the frequency step applied to the LPLL is smaller than the pull-in range, the loop locks again after a short time.

Finding the Pull-in Frequency (Frequency step = 7000Hz)



The frequency step of 7000Hz causes the LPLL to pull-out again. However, the pull-in process takes longer than before.

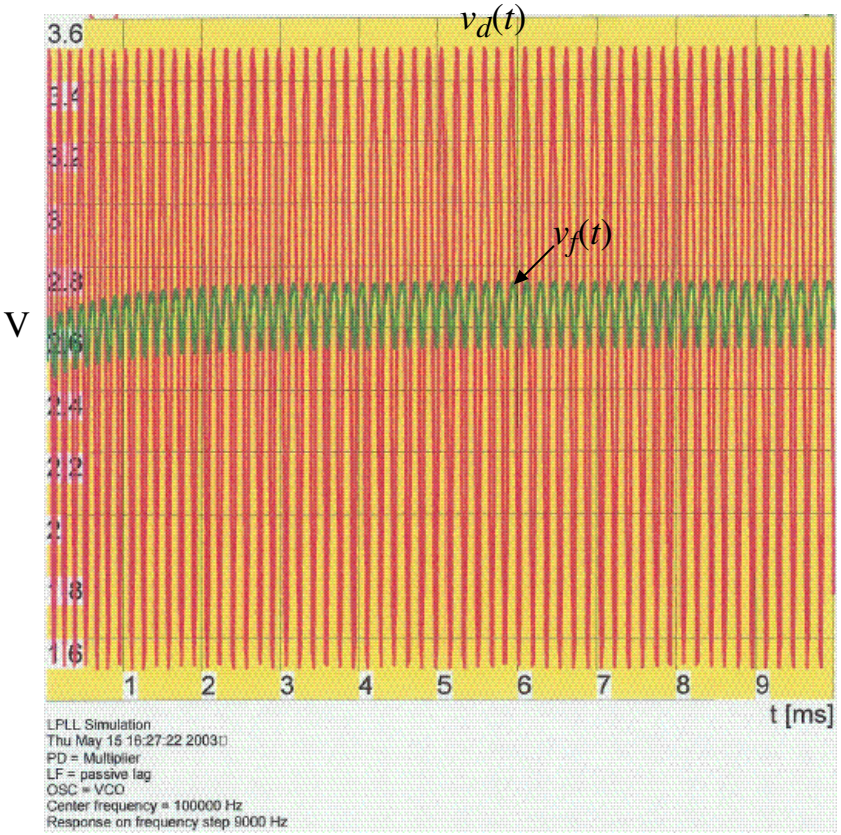
Finding the Pull-in Frequency (Frequency step = 8000Hz)



The frequency step of 8000Hz causes the LPLL to pull-out again. However, the pull-in process takes even longer than before.

We can estimate the lock range by observing that $v_f(t)$ gets slowly "pumped up". When it reached about 2.8V, the PLL became locked within one oscillation of $v_d(t)$. The value of $v_f(t)$ at lock is 2.9V. The 0.1V difference corresponds to a lock range of 2000Hz.

Finding the Pull-in Frequency (Frequency Step = 9000Hz)



The frequency step of 9000Hz causes the LPLL to pull-out and is no longer able to pull back in.

Further simulation showed that the LPLL cannot pull back in for a frequency step of 8500Hz.

$\therefore$ The pull-in frequency is near 8500Hz compared with a predicted value of 8534Hz.

SUMMARY

- Lectures 050 and 060 constitute a systems perspective of the LPLL
- LPLL components are:
  1.) Multiplying phase detector
  2.) Low pass filter
  3.) Voltage controlled oscillator
- Locked state: Input frequency = VCO frequency
  The phase response is low pass
  The phase error response is high pass
- Unlocked state:
  - Hold range ($\Delta\omega_H$) – frequency range over which a PLL can statically maintain phase
  - Pull-in range ($\Delta\omega_P$) - frequency range within which a PLL will always lock
  - Pull-out range ($\Delta\omega_{PO}$) – dynamic limit for stable operation of a PLL
  - Lock range ($\Delta\omega_L$) - frequency range within which a PLL locks within one single-beat note between reference frequency and output frequency
- The order of a PLL is equal to the number of poles in the open-loop PLL transfer function
- LPLL design –Design the parameters K_o, K_d, ζ, and the filter $F(s)$ of the LPLL for a given performance specification.

