Fully Integrated Low Phase Noise LC VCO

AGENDA

- Comparison with other types of VCOs.
- Analysis of two common LC VCO topologies.
- Design procedure for the cross-coupled LC VCO.
- Phase noise reduction techniques.

Desired Characteristics of VCOs

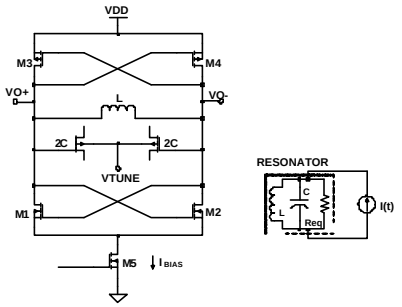
- Low phase noise.
- Wide tuning range.
- Low cost (i.e. compatible with IC process).
- Small size.
- Low power consumption.

Comparison of various types of VCOs

Resonator Type	Frequency Range	Quality Factor	Tuning Range	Cost
LC (integrated)	500 MHz – 10 GHz	3 - 10	Wide	Very low
LC (discrete)	100 MHz – 1 GHz	50 – 100	Wide	Low
Quartz crystal	1 MHz – 500 MHz	10000 – 100000	Very narrow	High
Ceramic	3 KHz – 20 MHz	500 – 5000	Very narrow	Low
Transmission line	> 100 MHz	1000 – 5000	Wide	Moderate
Surface Acoustic Wave (SAW)	100 MHz – 2 GHz	30 – 400	Narrow	High
Dielectric (DRO)	2 GHz – 30 GHz	About 12000	Narrow	Moderate

- Only LC and transmission line VCOs are suitable for IC process.
- Transmission lines have higher Q but are much larger than spiral inductor.

Complimentary Cross-Coupled LC VCOs



(a) Complimentary cross-coupled LC VCO

(b) Equivalent Circuit

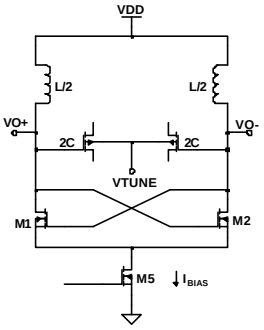
- Easy to design.
- Power efficient since bias current is shared between the two transconductors.
- Not suitable for low-voltage design due to voltage drop of bias transistor.

For operation in current-limited regime:

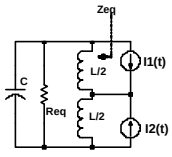
$$VO = \frac{4}{p} \cdot I_{BIAS} \cdot R_{EQ} \quad \text{(Ideal switching)}$$

$$VO \approx I_{BIAS} \cdot R_{EQ} \quad \text{(High frequency)}$$

Singly cross-coupled LC VCO



(a) Singly cross-coupled LC VCO



(b) Equivalent Circuit

By superposition:

$$VO = 2 \cdot I1(t) \cdot Z_{eq} \cdot \frac{R_{eq} // 1/jwC}{R_{eq} // 1/jwC + jwL/2}$$

$$Z_{eq} = \frac{jwL}{2} // \left(\frac{jwL}{2} + R_{eq} // \frac{1}{jwC} \right)$$

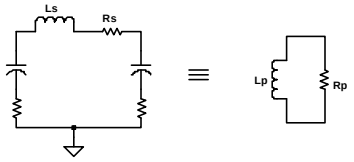
Simplifying using the identity $w^2 = \frac{1}{LC}$

$$VO = I1(t) \cdot R_{eq} = \frac{2}{p} \cdot I_{BIAS} \cdot R_{EQ}$$

Singly cross-coupled LC VCO in general has poorer phase noise performance than the complimentary one.

Design Procedure for cross-coupled LC VCO

1. Use design tool such as ASITIC to obtain the ? model of the spiral inductor.
2. Convert to parallel equivalent, assuming Q>>1.
3. Estimate VCO output swing V_O. V_{DS5} should be chosen to be about 4 times $V_{DS5(sat)}$ to minimize noise up-conversion by the bias transistor.
4. Compute the bias current, assuming the resonator Q is dominated by the inductor Q.



$$L_S = \frac{L_P R_P^2}{R_P^2 + w_0^2 L_P^2} \approx L_P$$

$$R_S = \frac{w_0^2 L_P^2 R_P}{R_P^2 + w_0^2 L_P^2} \approx \frac{w_0^2 L_P^2}{R_P}$$

$$V_O = V_{DD} - V_{TP} - V_{TN} - V_{DS5}$$

$$I_{BIAS} \approx \frac{V_O}{R_P}$$

Design Procedure for cross-coupled LC VCO

5. Compute the W/L of the two trans-conductors, assuming that the negative resistance is equally divided between them, and the magnitude of the total negative resistance is equal to 1/3 of R_P for reliable startup.
6. Compute C to get the desired oscillation frequency.

$$\frac{2}{g_m} = 2 \cdot \frac{R_P}{3}$$

$$\frac{1}{\sqrt{2k'\frac{W}{L}I_D}} = \frac{R_P}{3}$$

$$\frac{1}{\sqrt{k'\frac{W}{L}I_{BIAS}}} = \frac{R_P}{3}$$

$$C = \frac{1}{w_0^2 L}$$

Design Example

Problem:

Design a 5.5-GHz complimentary cross-coupled LC oscillator, given that L_S=1.26nH, R_S=4.25, V_{DD}=1.8V, V_{TN}=0.2V, V_{TP}=0.25V, k_N'=170µA/V, k_P'=75µA/V, and $V_{DS5(sat)}$=0.17V

Answer:

I_{BIAS}=1.502mA, $(W/L)_1$=177, $(W/L)_3$=401, $(W/L)_5$=611, C=664.6fF

Notes:

The actual bias current and capacitance should be less than the calculated values, due to parasitic capacitance of the transistor.

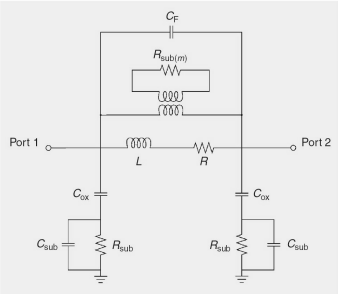
Phase Noise Reduction Techniques

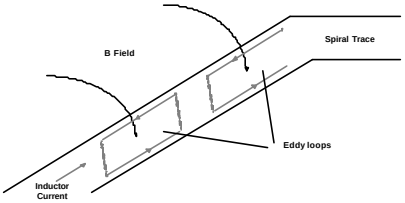
Phase noise can be reduced by:

1. Increasing the Q of the LC tank, i.e. better design techniques for planar inductor and varactor.
2. Increasing the output voltage swing.
3. Reducing the effect of the bias transistor 1/f noise up-conversion.
4. Reducing transistor noise.

T. H. Lee, and A. Hajimiri, "Oscillator Phase Noise: A tutorial", IEEE J. Solid State Circuits, vol. 35, no. 3, pp. 326-335, Mar. 2000
T. H. Lee, and A. Hajimiri, "Design Issues in CMOS Differential LC Oscillators", IEEE J. Solid State Circuits, vol. 34, no. 5, pp.717-724, May 1999

Spiral Inductor Losses





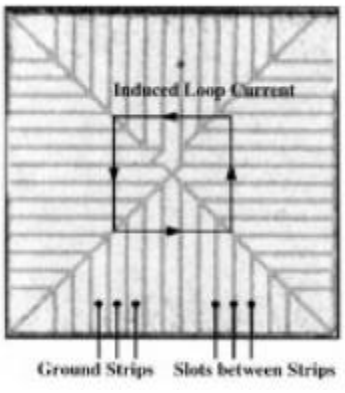
- Metal trace resistance, increased at high frequency due to skin effect and current crowding effect.
- Parasitic capacitance between metal trace and substrate.
- Magnetic field coupling to the substrate, causing image current to flow in the substrate (Faraday's law).

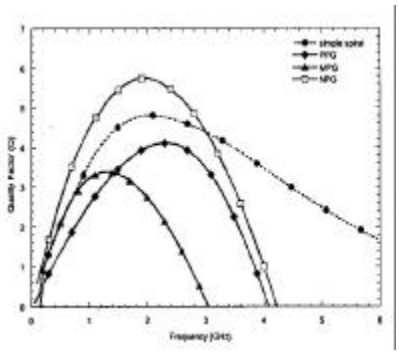
High-Q Spiral Inductor Design Techniques

(a) (b)

- Limit the width of the metal conductors.
- Use minimum spacing in between the conductors.
- Do not fill the inductor up to the center.
- Limit the area occupied by the coil.
- Use octagonal shape to minimize trace metal resistance.
- Shunt multiple metal layers to reduce trace resistance.
- Use pattern ground shield.

Pattern Ground Shield



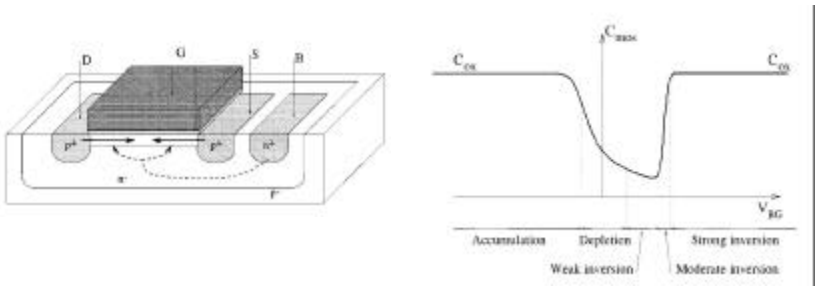


- The effectiveness of pattern ground shield is questionable. Only N+ diffusion shield shows some improvement, but only for frequency below 3 GHz.

Reverse Biased p-n Junction Varactor

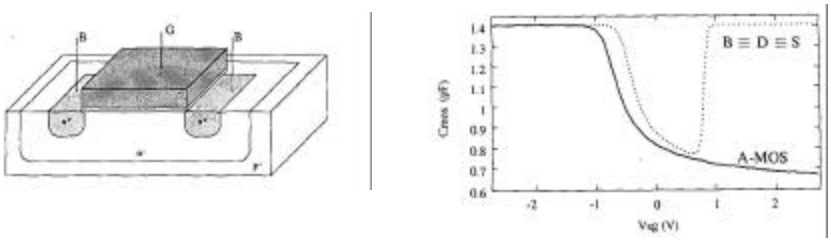
- Does not scale with technology.
- Have limited tuning range, typically less than ½ supply.
- Have relatively high parasitic series resistance.

MOS Varactor



- Have larger capacitance/area ratio than p-n junction varactor.
- Have larger tuning range than p-n junction varactor.
- Have lower parasitic resistance than p-n junction varactor.
- Scale with technology.

Accumulation-mode Varactor

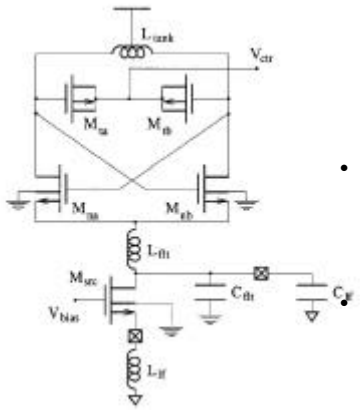


- Can be constructed as a pMOS transistor with the D/S p+ diffusions removed, to suppress any injection of holes into the channel, thereby eliminating the formation of inversion region.
- Have lower parasitic resistance than a MOS varactor since electrons are the majority carriers.

Phase Noise Contribution of Varactor

- Noise appearing on the varactor terminals, will vary the CM signal which, in turn, varies the capacitance which is translated to phase noise at the VCO output.
- This problem can be alleviated by utilizing an array of fixed switched capacitance, in parallel with a much smaller varactor. The drawback is the on resistance of switching transistors will degrade the Q of the resonator.
- Another approach is to use an array of smaller varactors, with all but one discretely switched between two extremes of the varactor tuning range.

Tail Current Noise Suppression



- High frequency noise of the tail current transistor is suppressed by C_{flt}. L_{flt} is chosen to resonate at the second harmonic, thereby preserving the high impedance at the drain of the tail current transistor.
- A large external inductor L_{lf} is used to degenerate the tail transistor, reducing the low frequency noise power by $\left|1+jg_m wL_{fl}\right|^2$.
- An external capacitor can be used in place of the inductor, but it also provides a low impedance for the common source of the switching transistors.