asQED Symposium 2011

A Novel and Fast Method for Characterizing Noise Based PCMOS Circuits

Anshul Singh[1], Satyam Mandavalli[1],
Vincent J Mooney[2,3,4], Keck Voon Ling[3]

20th July 2011

[1]CVEST, International Institute of Information Technology, Hyderabad, India
[2]School of ECE, Georgia Institute of Technology, Georgia, USA
[3]School of EEE, Nanyang Technological University, Singapore
[4]School of Computer Engineering, Nanyang Technological University, Singapore

asQED Symposium 2011

Outline

- **Introduction**
- Prior Work
- A Quick Method for Characterizing PCEs
  - Noise Characterization
  - Dynamic Noise Analysis
  - Error-Rate Calculation
  - Simulation Results
- Conclusion

asQED Symposium 2011

Introduction

- Decreasing feature size of CMOS transistors
  - Increasing statistical behavior
- Growing energy concerns
- Probabilistic Computing
  - Allows occasional errors in computation
  - Trades reliability with the traditional three parameters of circuit design: energy, speed and area.

asQED Symposium 2011

Error-Rate Prediction

- The most important information about probabilistic circuits: output error-rate.
- For systematic design and performance evaluation of probabilistic circuits quick and accurate error-rate prediction is crucial.
- General idea for prediction methodologies:
  - Obtain error-rates of constituent probabilistic circuit elements, process known as characterization of probabilistic circuit elements.
  - Use mathematics to model error generation and propagation mechanisms through circuit elements.

asQED Symposium 2011

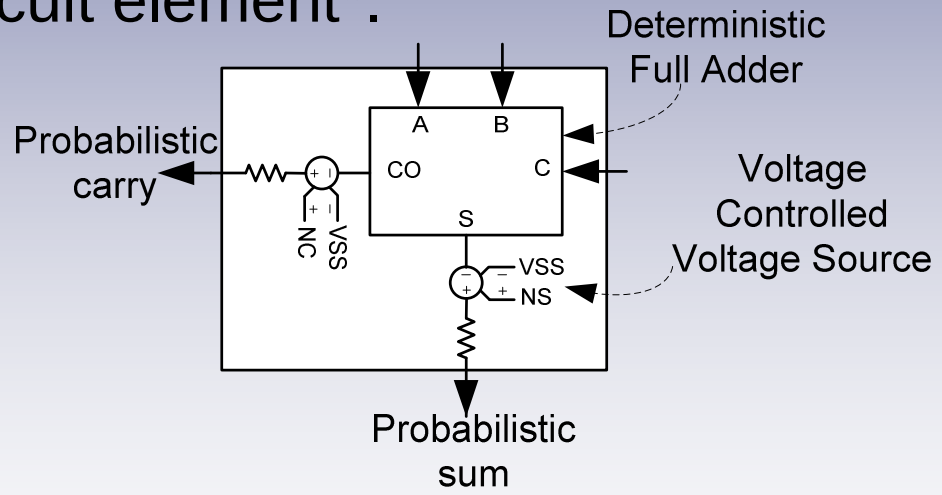
Outline

- Introduction
- **Prior Work**
- A Quick Method for Characterizing PCEs
  - Noise Characterization
  - Dynamic Noise Analysis
  - Error-Rate Calculation
  - Simulation Results
- Conclusion

asQED Symposium 2011

Modeling Future Noisy Probabilistic Circuit Elements

- A noisy probabilistic circuit element is modeled
  - by adding equivalent noise sources at the outputs of the deterministic version of the circuit element or non-noisy circuit element*.



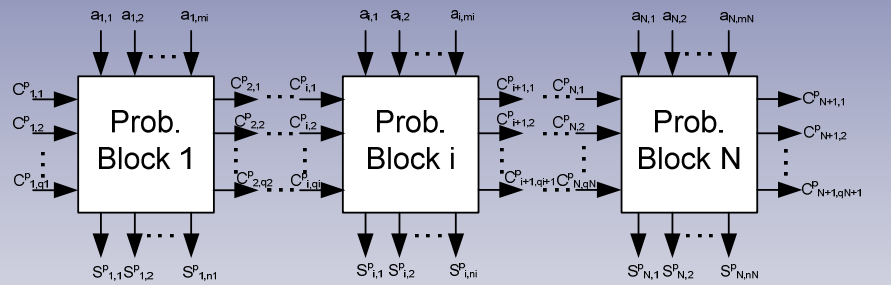
A Probabilistic FA Built from a Deterministic FA

* P. Korkmaz, B. E. S. Akgul, L. N. Chakrapani, and K. V. Palem, “Advocating noise as an agent for ultra low-energy computing: Probabilistic CMOS devices and their characteristics,” Japanese Journal of Applied Physics, vol. 45, pp. 3307–3316, Apr. 2006.

asQED Symposium 2011

Error-Rate Prediction Methodology: The Cascade Math Model

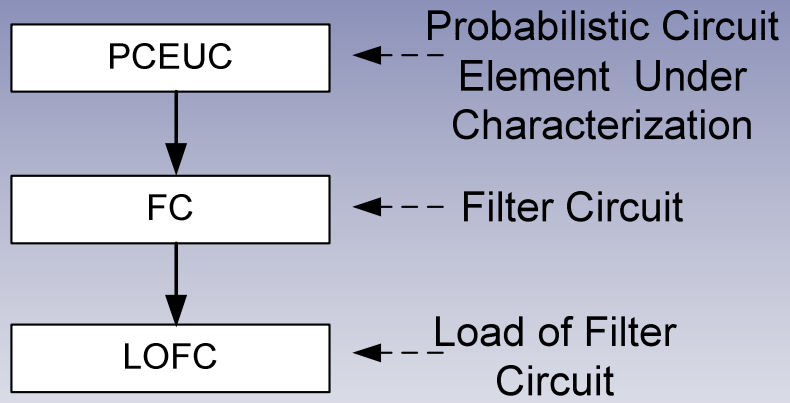
- Lau et al. have come up with a methodology to quickly predict the error-rates of cascade structure of blocks*.
- The methodology is based on
  - Knowing each block's output error-rate
  - Evaluation of mathematical equations that model the dynamics of error generation and propagation across the blocks.



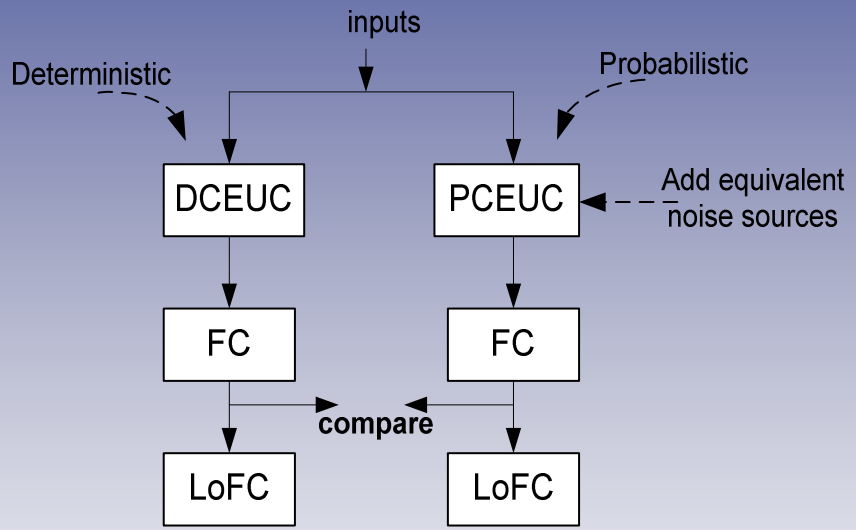
Cascade Structure of Blocks

*M. Lau, K. V. Ling, A. Bhanu, and V. J. Mooney III, "Error Rate Prediction for Probabilistic Circuits with More General Structures", The 16th Workshop on Synthesis And System Integration of Mixed Information technologies" (SASIMI2010), 18-19 October, 2010, Taipei, Taiwan, pp.220-225

Characterizing PCEs – The Three Stage Model*



The Three Stage Model



Experimental Setup

*Anshul Singh, Arindam Basu, Keck-Voon Ling and Vincent J. Mooney III, "Modeling multi-output filtering effects in PCMOS," VLSI-DAT, April 25-27, Hsinchu, Taiwan, pp. 414-417, 2011.

asQED Symposium 2011

Outline

- Introduction
- Prior Work
- **A Quick Method for Characterizing PCEs**
  - Noise Characterization
  - Dynamic Noise Analysis
  - Error-Rate Calculation
  - Simulation Results
- Conclusion

asQED Symposium 2011

Characterizing PCEs

- The characterization procedure discussed, requires simulation of the three stage model for large number of samples.
  - computationally intensive, requiring large computation time
- Characterizing PCE.
  - Measure of the number of actual errors that are caused at the output of PCE.
  - Looking at the characterization procedure from the point of view of Filter circuit's
    - Noise Tolerance of filter circuit

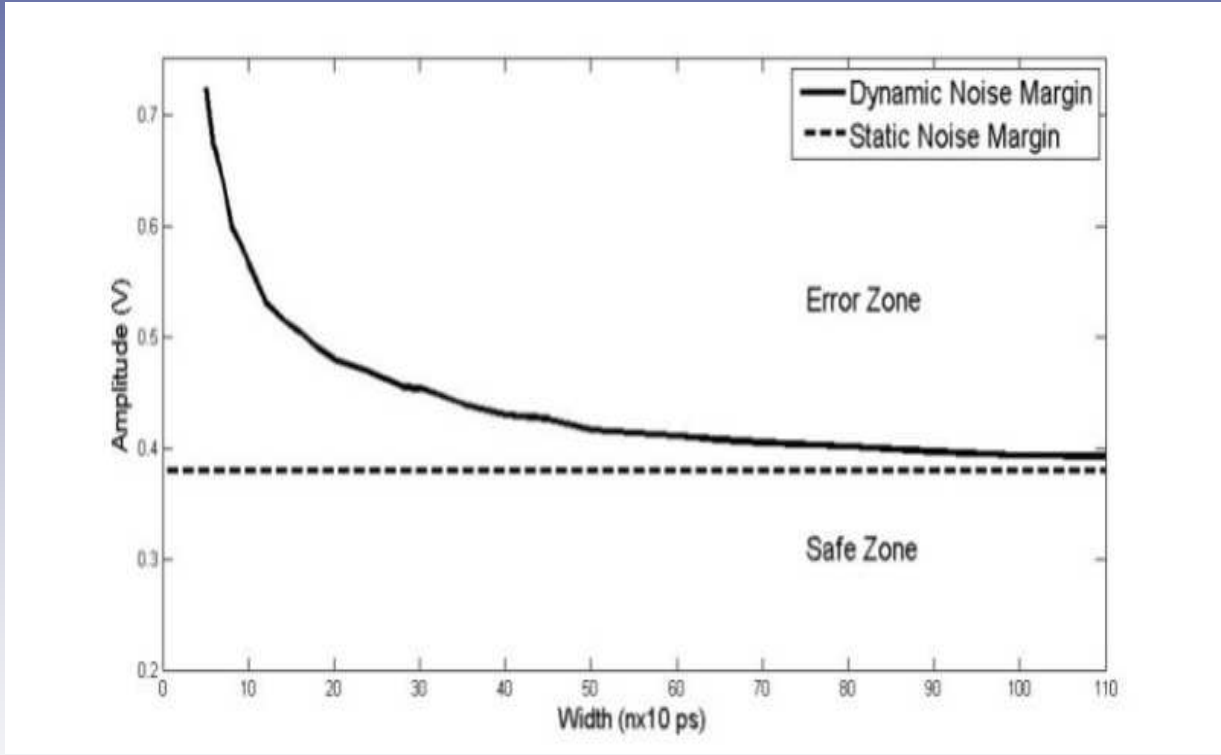
asQED Symposium 2011

Noise Margin

- Noise margin gives the measure of noise amplitude that can be tolerated by a circuit without affecting its correct operation
- Two types of noise analyses
  - Static Noise Analysis
    - treats noise as a DC signal
  - Dynamic Noise Analysis
    - noise margin for pulses

asQED Symposium 2011

Static vs. Dynamic Noise Margin



Static and Dynamic Noise Margin of an Inverter*

*** 90nm Synopsys generic library, operating at 0.8V**

asQED Symposium 2011

A New Approach

- Perform Dynamic Noise Analysis (DNA) on the three stage model of a PCE through SPICE simulation
  - computationally very cheap.
- Perform a new statistical analysis on time domain noise, structural analysis, to calculate error-rate from DNA on FCs of the three stage model of PCEs.
- Combine the above two information to obtain error-rates of PCEs.

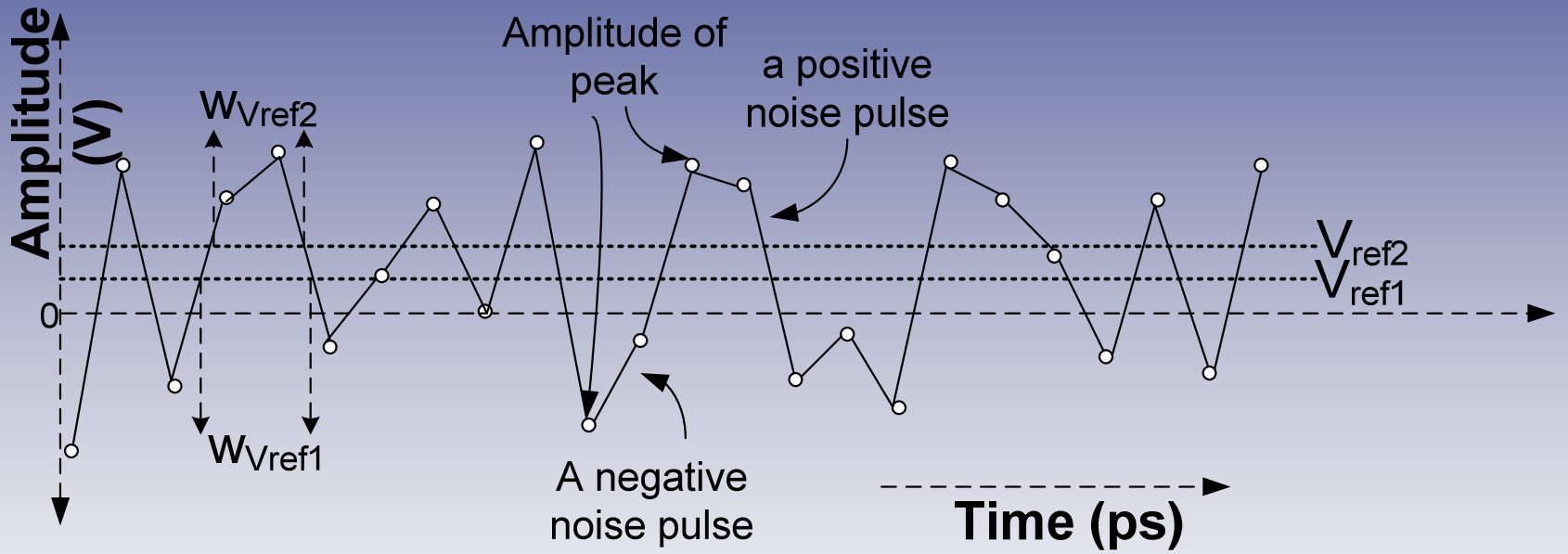
asQED Symposium 2011

Structural Analysis of Noise

- Static noise margin
  - Considers only amplitude of noise before declaring a potential error creator.
    - Amplitude distribution of time domain noise.
- Dynamic Noise Analysis
  - Takes into account the amplitude and the duration/width of noise pulses
- Information required from noise for error-rate calculation using DNA
  - Pulse Amplitude distribution
  - Pulse Width distribution
  - Amplitude-Width relation

asQED Symposium 2011

A Noise Sample



A Zero Mean Gaussian Noise

Noise is assumed to be continuous and linearly varying with time between two data points

asQED Symposium 2011

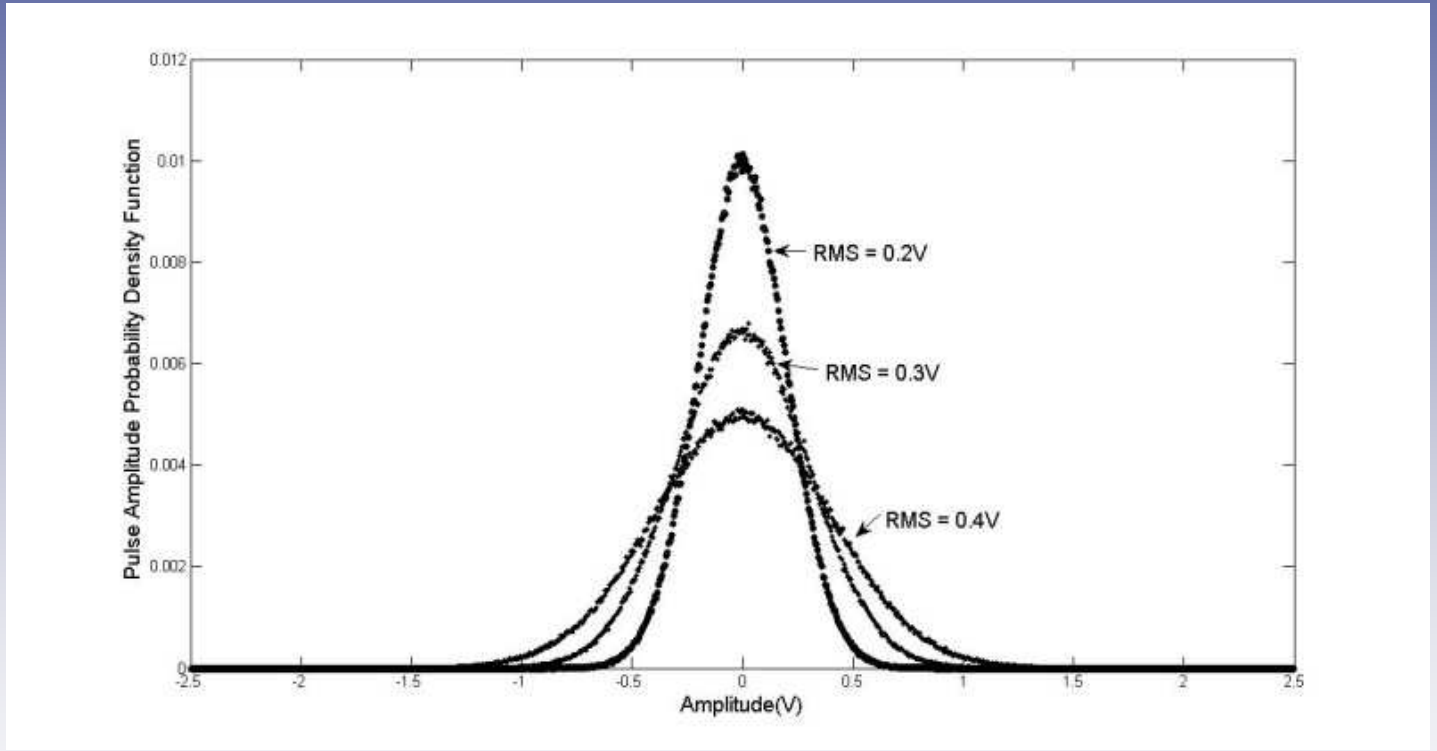
Amplitude Distribution

- Pulse Amplitude Probability Density Function (PAPDF) gives the probability that the amplitude of a pulse falls within certain amplitude range.
- Since the PAPDF of Gaussian noise follows a Gaussian distribution, it is given by function

$$a(V) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\left(\frac{(V-V_0)^2}{2\sigma^2}\right)}$$

asQED Symposium 2011

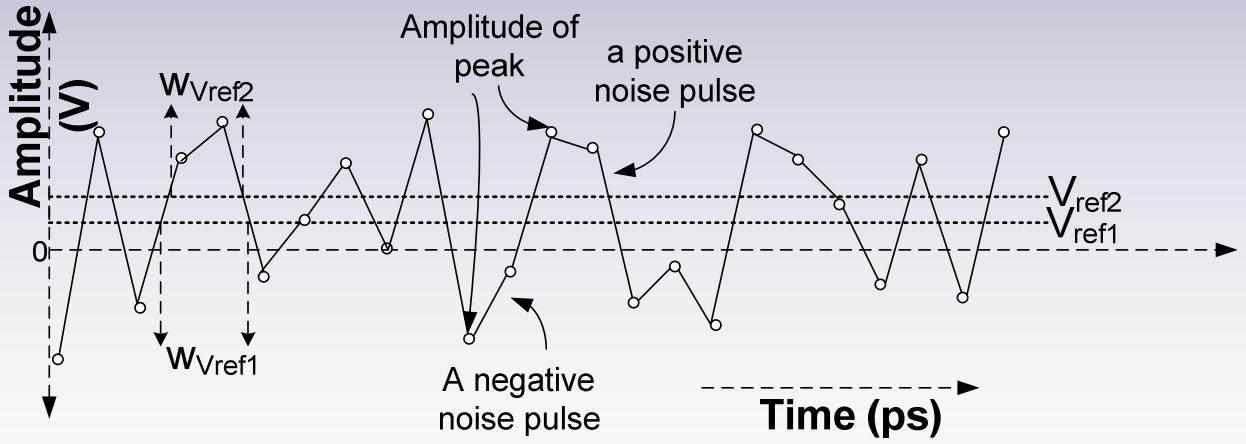
PAPDF



Pulse Amplitude Probability Density Function of Zero Mean Gaussian Noise

Pulse Width Distribution

- Pulse Width
  - the duration of a pulse at some reference voltage.
  - width distribution is defined for a reference voltage.



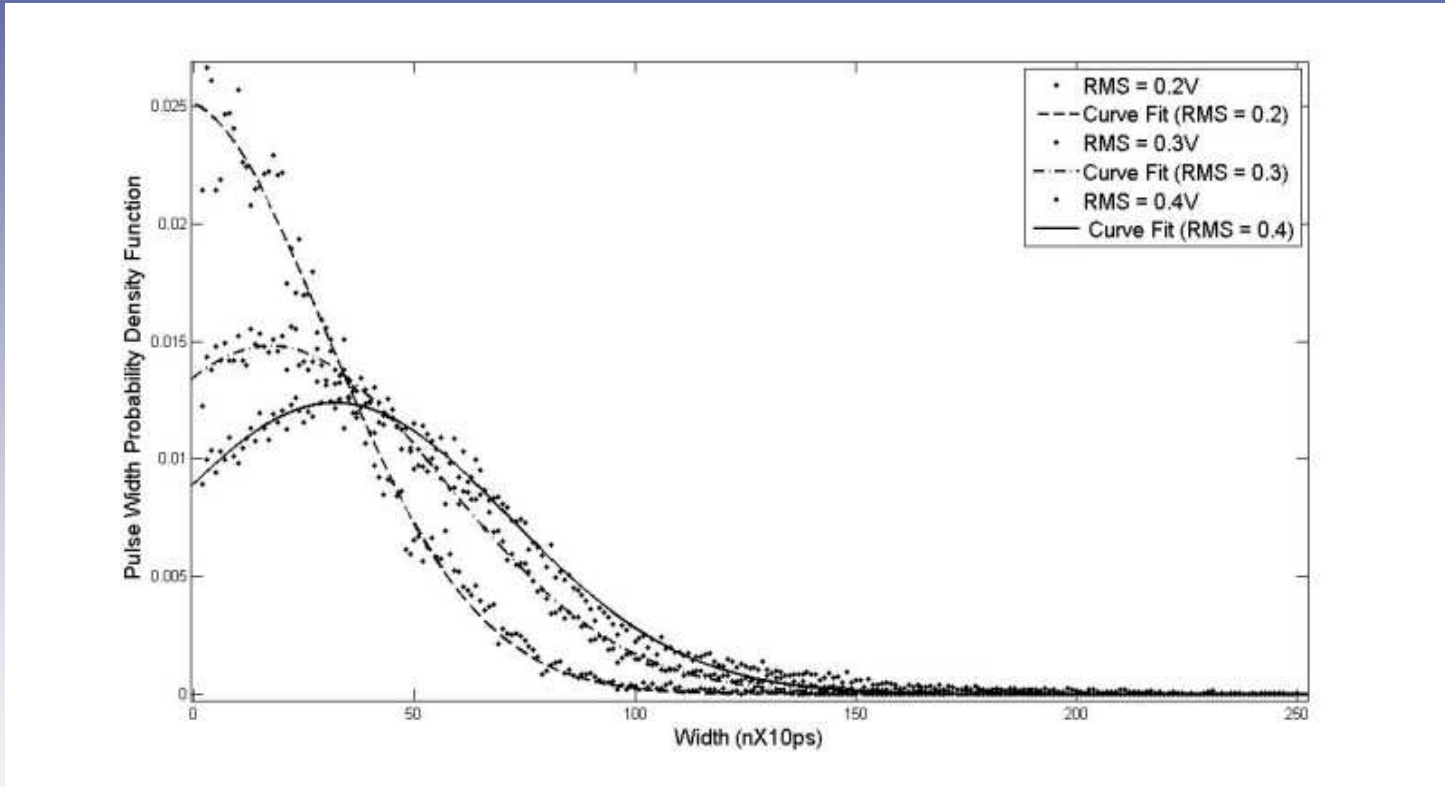
asQED Symposium 2011

PWPDF

- Pulse Width Probability Density Function (PWPDF) gives the probability that the width of a pulse falls within a certain range.
- Parameters affecting PWPDF
  - RMS value of noise
  - Reference Voltage

asQED Symposium 2011

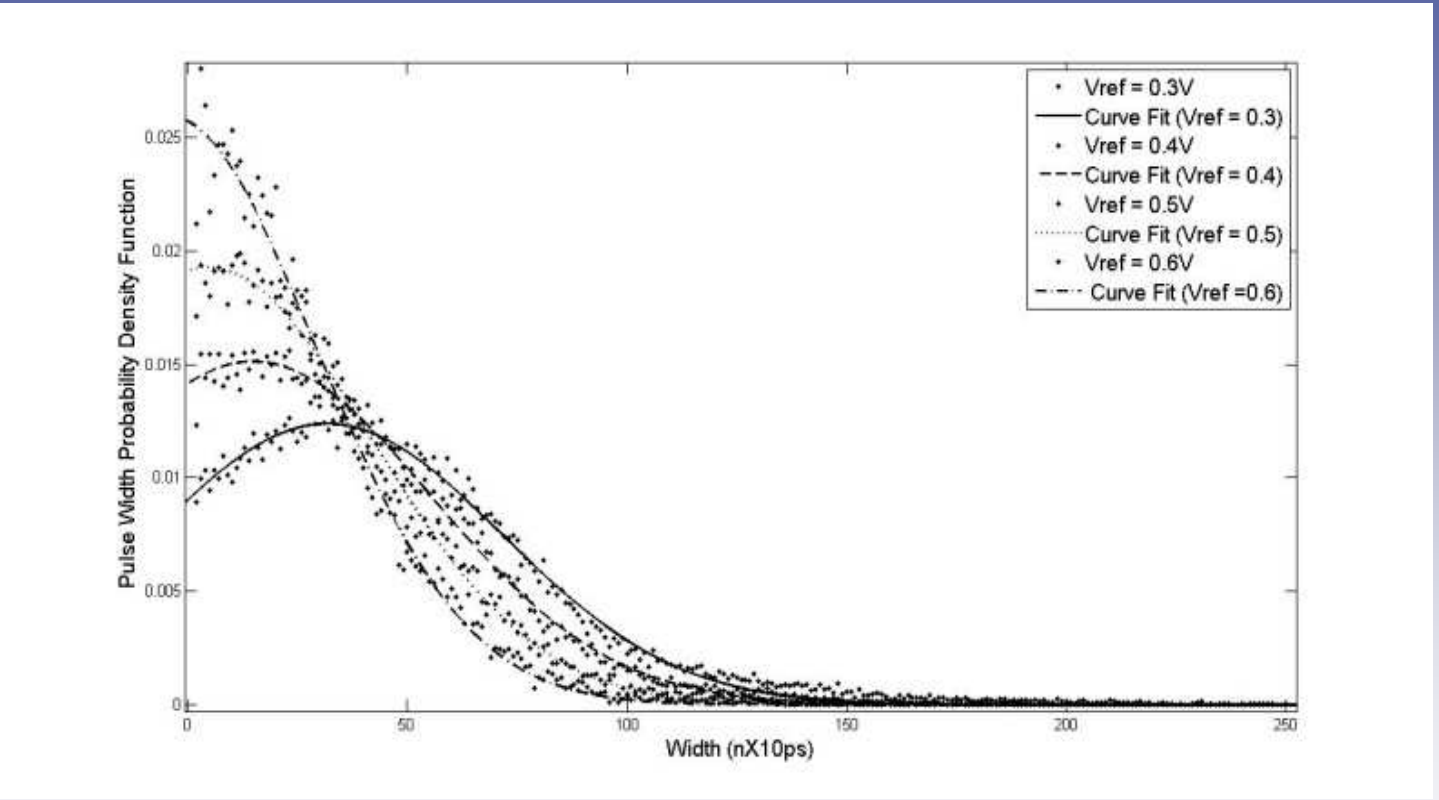
PWPDF and RMS



Dependence of PWPDF on RMS value

asQED Symposium 2011

PWPDF and Reference Voltage



Dependence of PWPDF on Reference voltage

asQED Symposium 2011

PWPDF: The Expression

- Using curve fitting techniques to obtain the PWPDF, we get

$$w(W) = ae^{-(W-b)^2/c^2}$$

  - Parameters a, b and c are constants for a particular RMS value and reference voltage, and W is the variable for width.
  - Parameters a, b and c have a polynomial relation with RMS and reference voltage.

asQED Symposium 2011

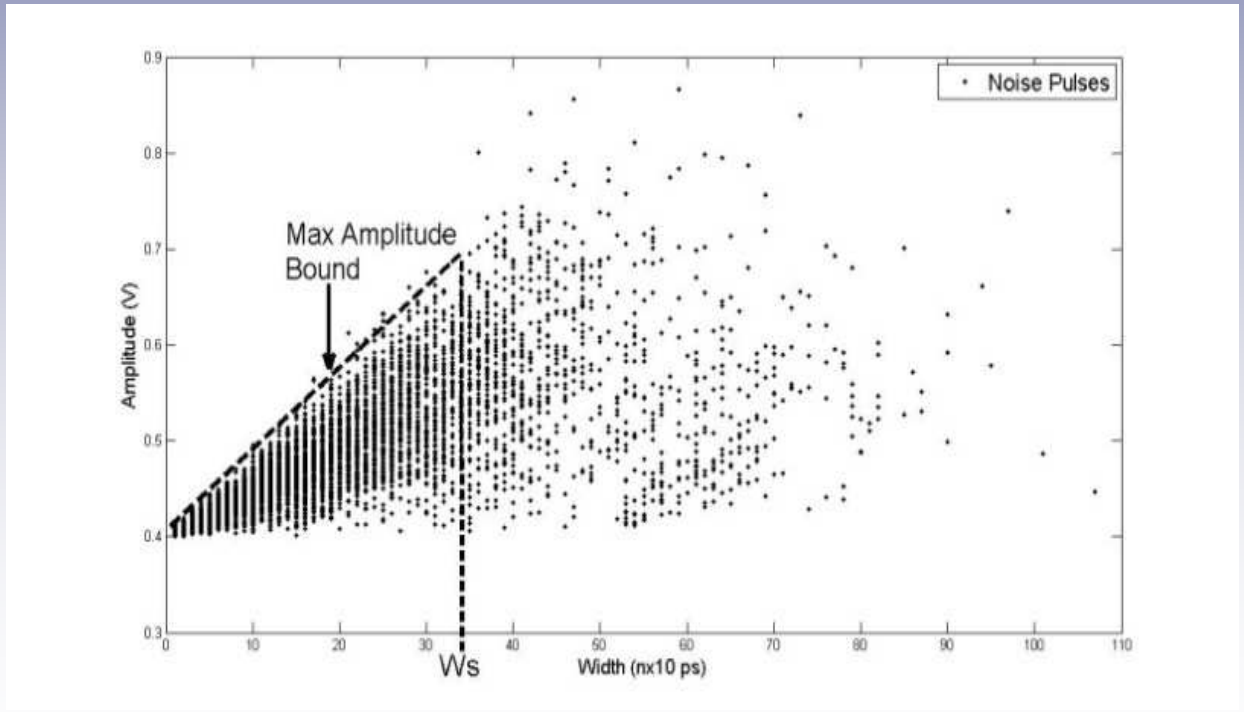
Joint Pulse Amplitude Width Density Function

- JPAWPDF is a function which gives the probability of a noise pulse to lie within a certain amplitude range and a certain width range.
  - sufficient information required to calculate error-rate.
- Obtaining JPAWPDF is a problem.
  - Either analytically from the amplitude and width distribution or using curve fitting techniques.

asQED Symposium 2011

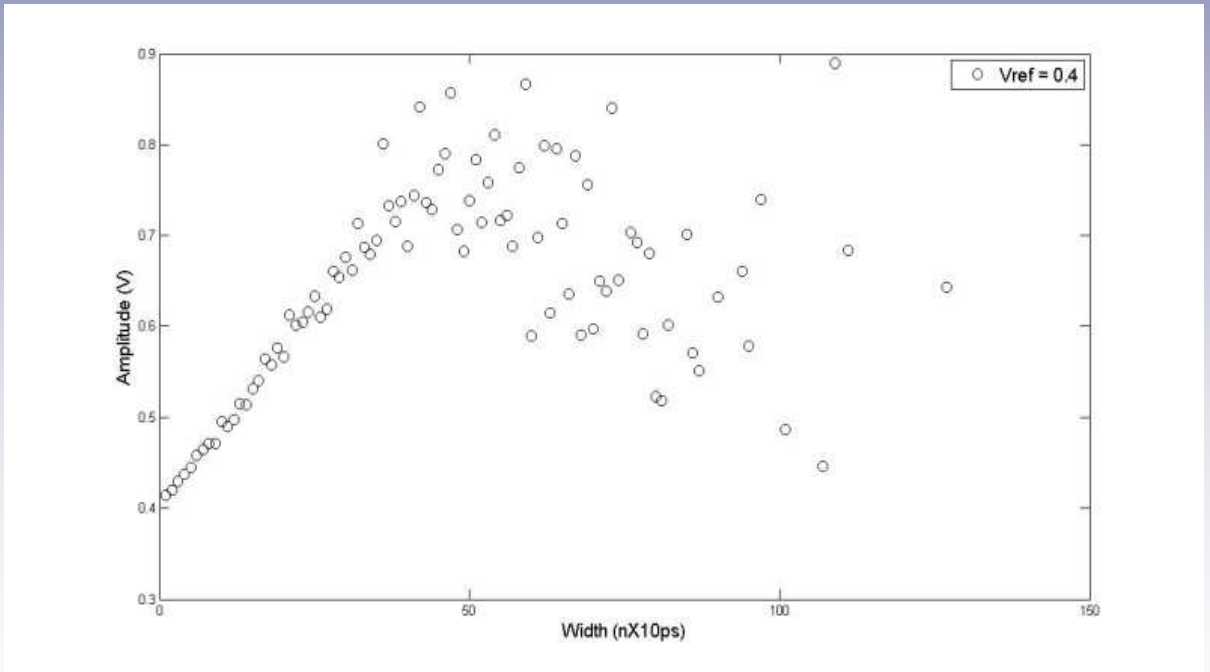
Amplitude-Width Relation: The Graphical Approach

- The amplitude-width relation relates the amplitudes of noise pulses with their widths.



Amplitude-Width Distribution of Gaussian Noise

- Noise pulses with smaller widths have maximum amplitudes below a certain bound.
- For larger widths such a condition does not hold true as the distribution becomes random.



Maximum Amplitude for each Width

asQED Symposium 2011

Max Amplitude per Width (MAW)

- For lower widths the max-amplitude shows a strong correlation with widths but becomes independent for higher widths.
- Parameters affecting MAW
  - RMS value of noise
  - Reference Voltage
- Expression obtained using curve fitting techniques

$$m(W) = pW + q$$

  - Constants p and q are polynomial function of RMS value and reference voltage, W is the variable for width

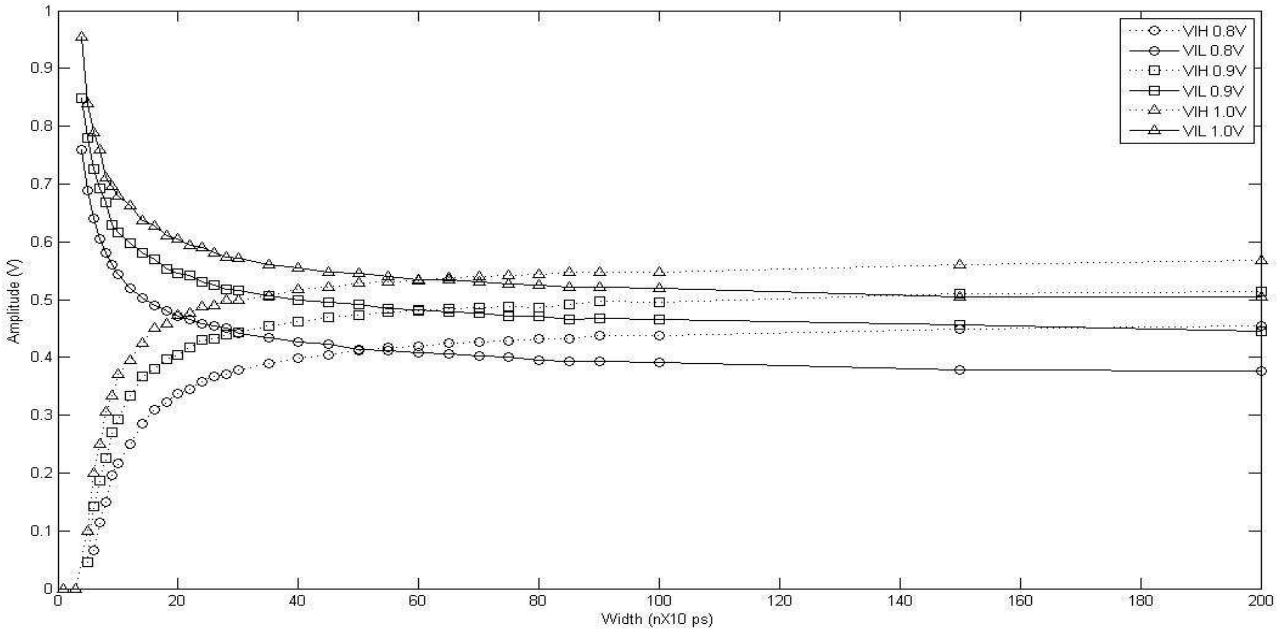
asQED Symposium 2011

Dynamic Noise Analysis (DNA)

- DNA gives the noise tolerance of logic gates
  - Considers noise pulse amplitude and width.
- DNA provides: V_{IL} and V_{IH} curves.
  - **V_{IL} curve**: the maximum voltage that can be considered as logic 0 by the gate when the input is going from logic 0 to 1 for different pulse widths.
  - **V_{IH} curve**: the minimum voltage that can be considered as logic 1 by the gate when the input is going from logic 1 to 0 for different pulse widths.

asQED Symposium 2011

V_{IL} and V_{IH} Curves



V_{IL} and V_{IH} Curves for an Inverter Operating at Different Voltages

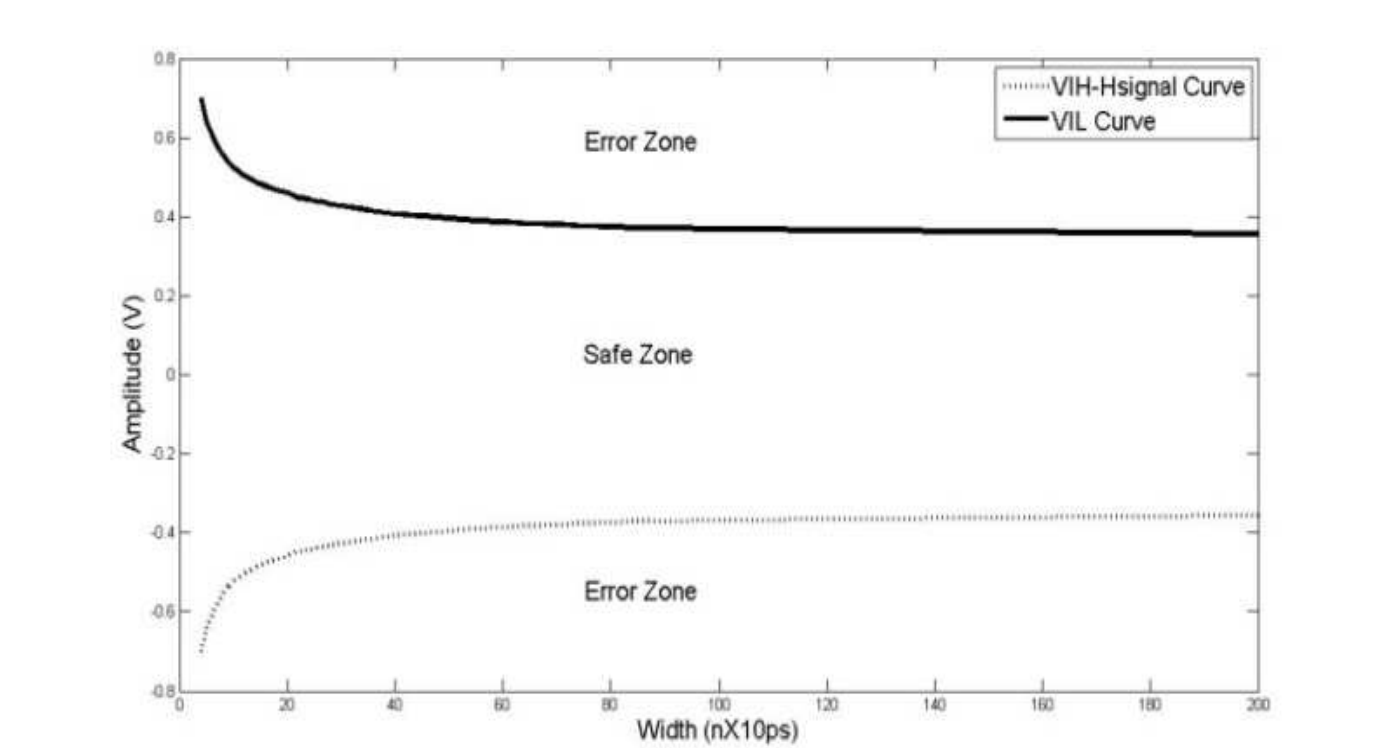
asQED Symposium 2011

Error Creation

- Positive noise pulses create 0 to 1 errors and negative noise pulses create 1 to 0 errors
  - 0(1) to 1(0) error: a signal which is at logic 0(1) but is treated as a 1(0) because of the noise present.
- A positive noise pulse, with width W_P, should have amplitude higher than that specified by V_{IL} curve for width W_P to potentially create a 0 to 1 error.
- To create a 1 to 0 error a negative noise pulse, with width W_N, should have amplitude lower than that specified by $V_{IH} – H_{signal}$ (V_{IH} minus H_{signal}) for width W_N.

asQED Symposium 2011

Error-Zone



V_{IL} and V_{IH} – H_{signal} Curves

asQED Symposium 2011

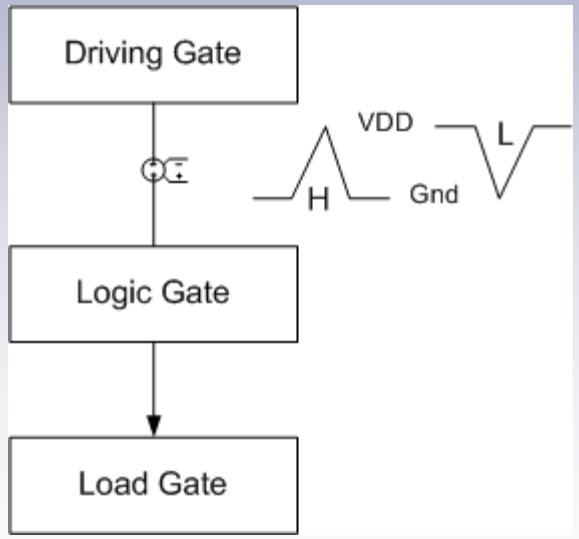
Obtaining V_{IL} and V_{IH} Curves

- V_{IL} and V_{IH} curves are obtained by SPICE simulations of logic gates.
  - Unity gain method
- V_{IL} and V_{IH} curves are obtained from Voltage Transfer Characteristics (VTC)of gates.
- V_{IL} and V_{IH} curves of a logic gate depends upon
  - The logic gate
  - The load of the logic gate
  - The driving gate

asQED Symposium 2011

Procedure

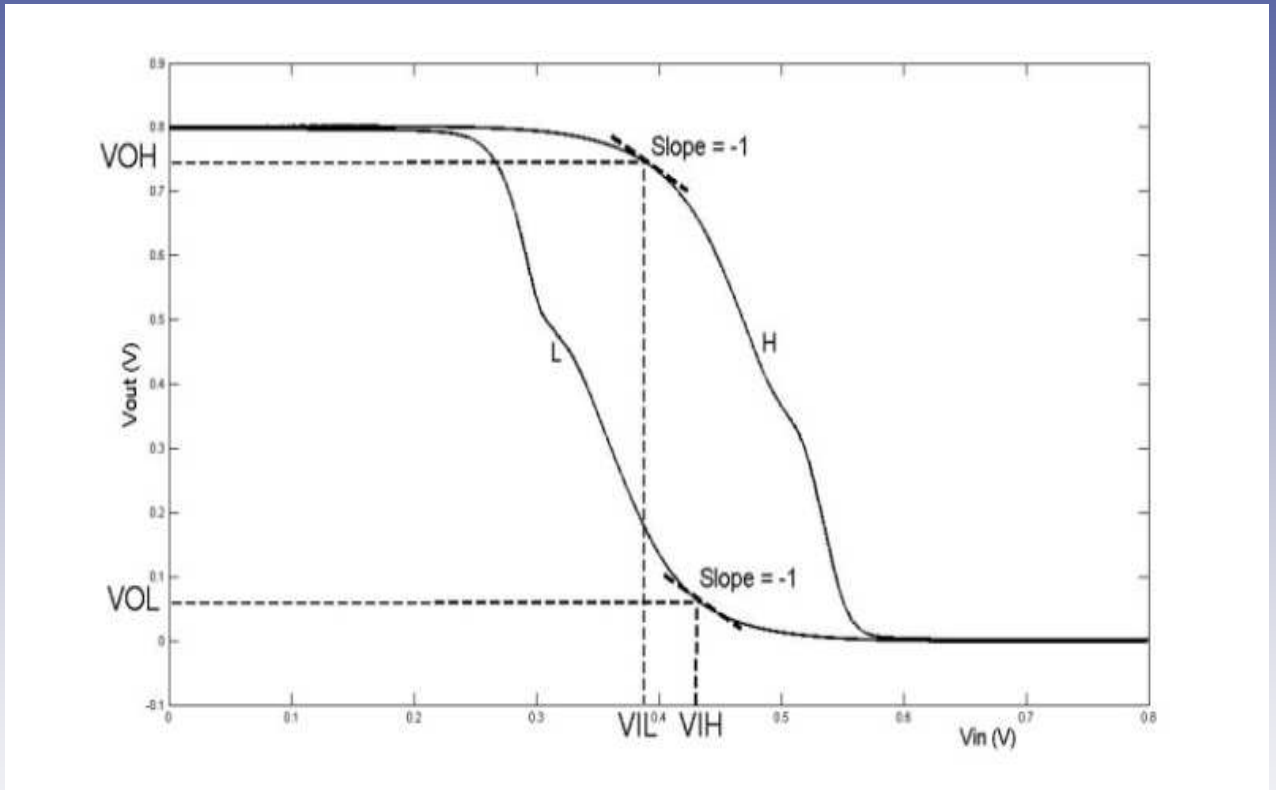
- Simulate the three stage model with a triangular input.
- Obtain VTC of logic gate using transient analysis.



Experimental Setup

asQED Symposium 2011

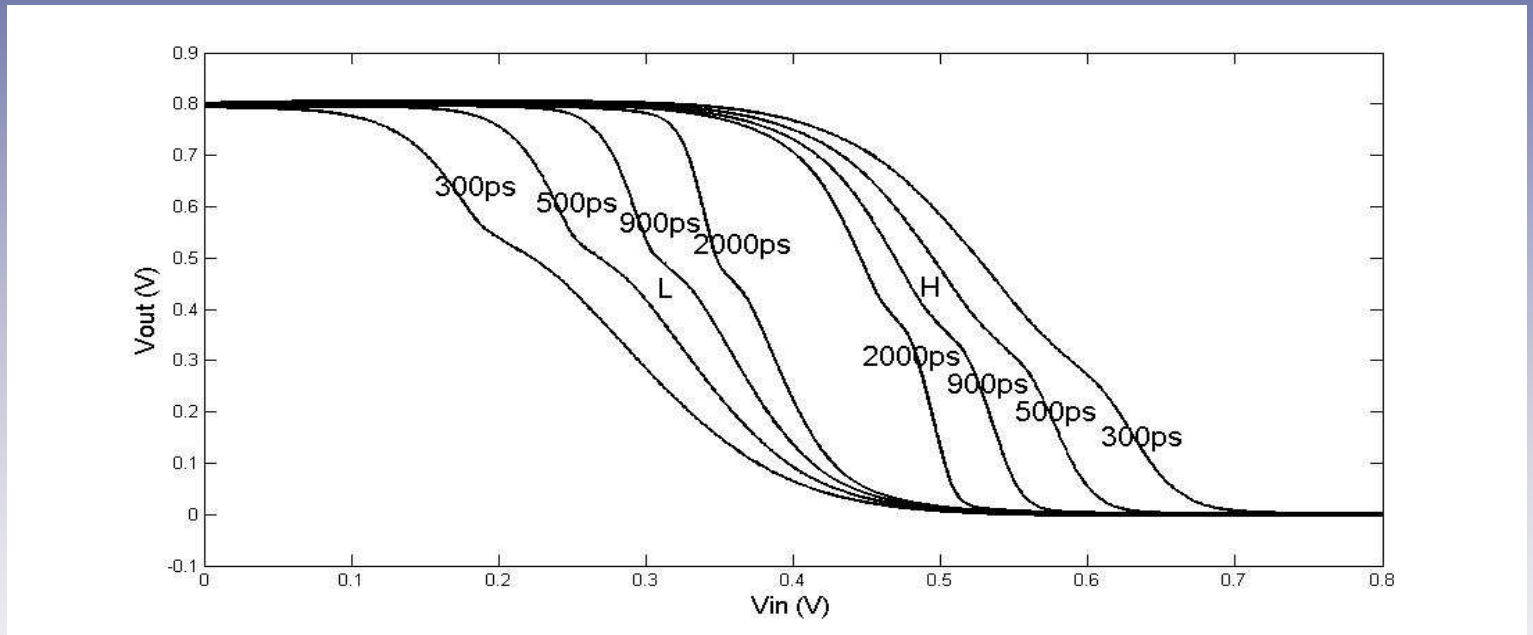
Unity Gain Approach



Unity Gain Approach for an Inverter

asQED Symposium 2011

Voltage Transfer Characteristics for Different Widths



Voltage Transfer Curve for Different Pulse Widths for an Inverter

asQED Symposium 2011

Representation of V_{IL} and V_{IH} Curve

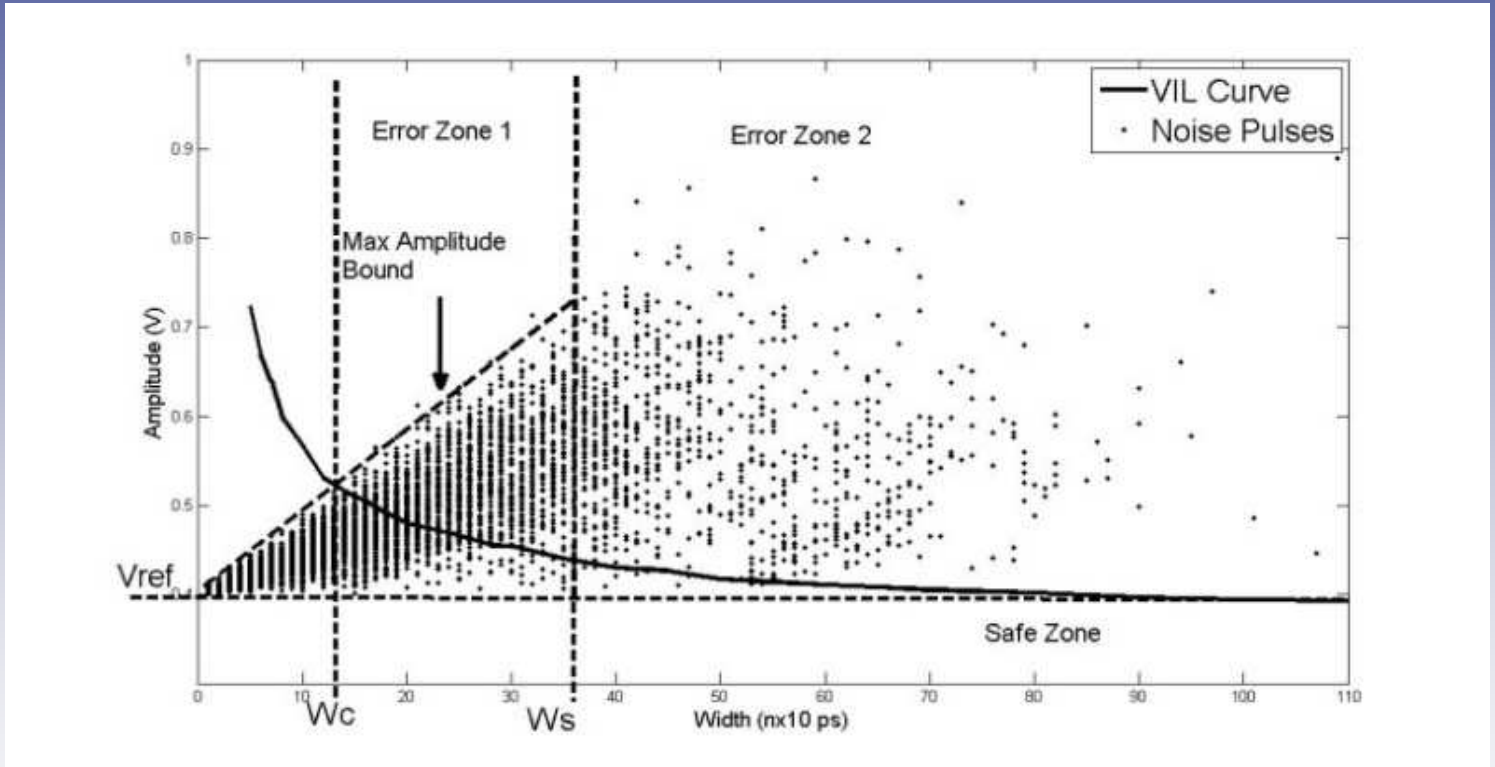
- V_{IL} and V_{IH} curves are represented by function $V_{IL}(W)$ and $V_{IH}(W)$,

$$V_{IL}/V_{IH}(W) = \frac{eW + f}{W + g}$$

- Parameters e, f and g are obtained from curve fitting and W is the variable for width.

asQED Symposium 2011

Error-Zone (0 to 1)



Error-Zone (0 to 1Errors)

asQED Symposium 2011

Error-Rate Calculation

$$e_1^H = \sum_{W_c^H+1}^{W_s^H} [w(W) * \int_{V_{IL}(W)}^{m(W)} a(V)dV]$$

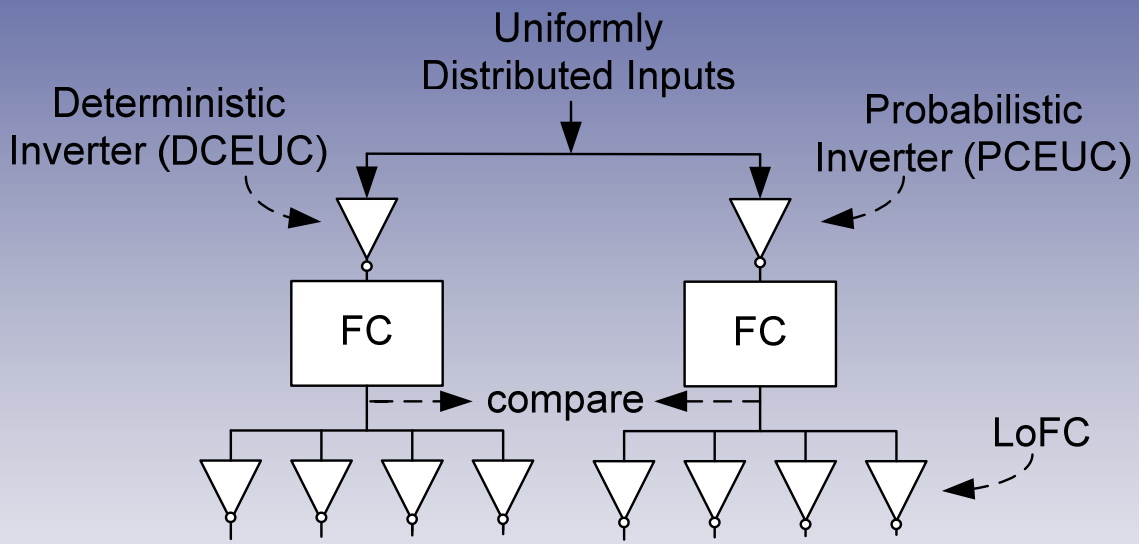
$$e_2^H = \sum_{W_s^H+1}^{W_{max}} [w(W) * \int_{V_{IL}(W)}^{\infty} a(V)dV]$$

$$e^H = e_1^H + e_2^H$$

- w(W) = PWPDF
- a(V) = PAPDF
- $V_{IL}(W) = V_{IL}$ curve
- m(W) = MAW
- W_c^H = crossover width
- W_s^H = max correlation width
- W_{max} = max width

asQED Symposium 2011

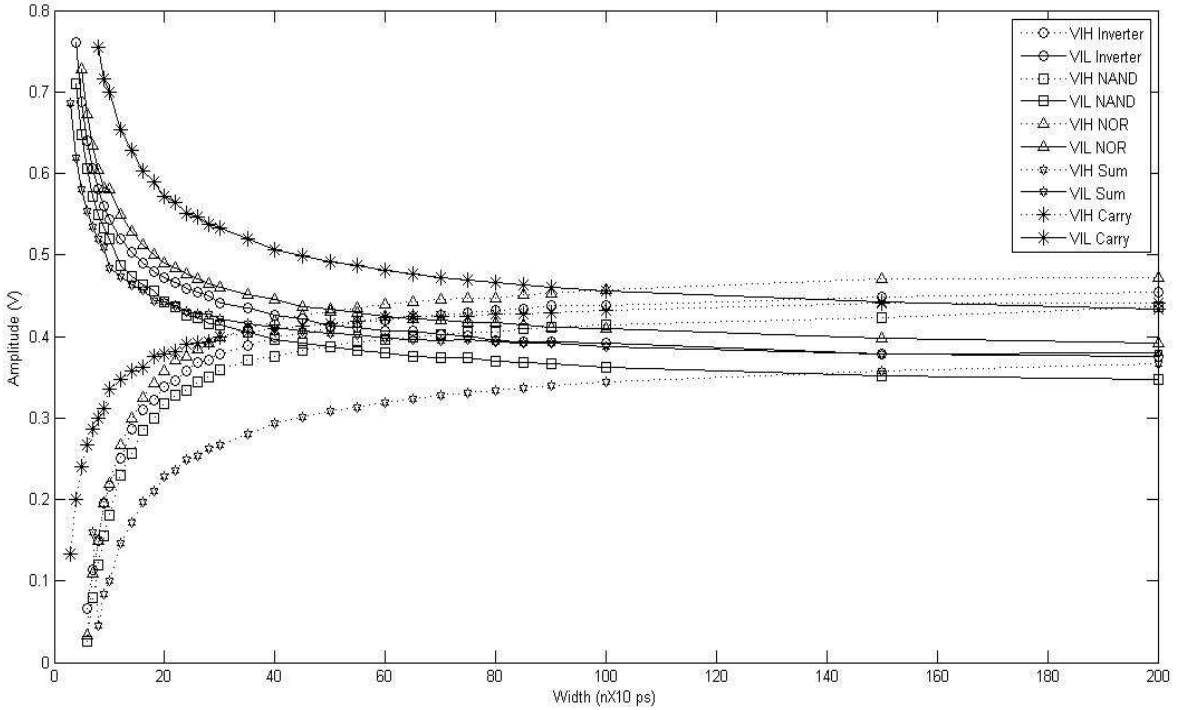
Simulations and Results



- FC: inverter, NAND, NOR, Full Adder

asQED Symposium 2011

V_{IL} and V_{IH} Curves



V_{IL} and V_{IH} Curves for Various Logic Gates

asQED Symposium 2011

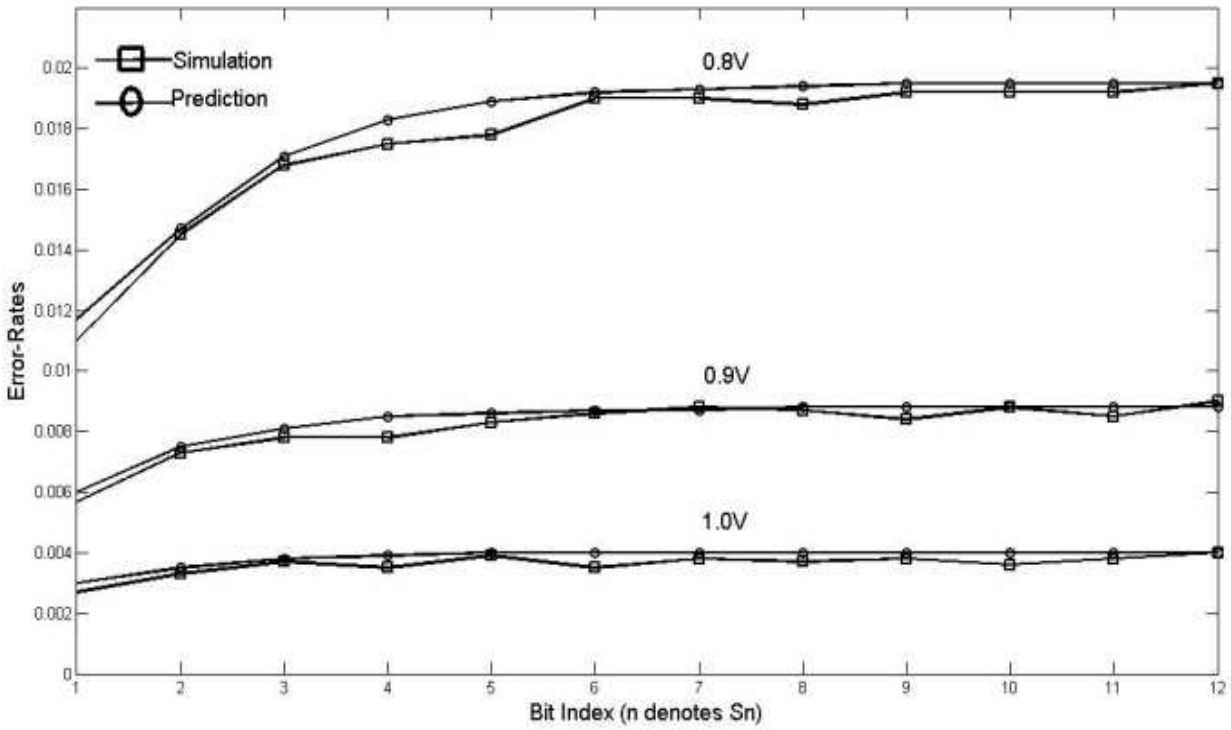
Results

	HSPICE Simulation						Prediction					
RMS	0.2 V			0.3 V			0.2 V			0.3 V		
VDD / Circuit Element	0.8 V	0.9 V	1.0V	0.8 V	0.9 V	1.0 V	0.8 V	0.9 V	1.0 V	0.8 V	0.9 V	1.0 V
Inverter	0.0109	0.0052	0.0022	0.0647	0.0452	0.0305	0.0113	0.0059	0.0024	0.0662	0.0468	0.0317
NAND	0.0112	0.0054	0.0026	0.0648	0.0454	0.0309	0.0117	0.0062	0.0030	0.0671	0.0473	0.0321
NOR	0.0105	0.0052	0.0023	0.0639	0.0449	0.0300	0.0112	0.0056	0.0025	0.0658	0.0464	0.0311
FA Carry (cin-cout')	0.0065	0.0030	0.0013	0.0519	0.0356	0.0235	0.0069	0.0033	0.0014	0.0536	0.0369	0.0245
FA Sum (cin-sum')	0.0047	0.0021	0.0009	0.0445	0.0306	0.0202	0.0050	0.0023	0.0010	0.0457	0.0324	0.0210

- Average relative deviation = 6%

asQED Symposium 2011

Probabilistic Ripple Carry Adder



Error-Rates of a 12-bit PRCA

- Using the Cascade Math Model and the results obtained from the new characterization procedure .
- Average relative deviation = 4.5%

asQED Symposium 2011

Simulation Time Comparison

Circuit Elements	Previous Approach (seconds)	Proposed Approach (seconds)
Inverter	483	7.2
NAND	618	7.2
NOR	620	7.8
Full Adder	1080	8.1

asQED Symposium 2011

Conclusion

- This work proposed structural analysis of time domain noise for effective representation of noise for error-rate estimation.
- A quick method of characterizing probabilistic circuit elements is proposed utilizing structural analysis of noise and dynamic noise analysis of the three stage model of PCEs.

asQED Symposium 2011

Publications

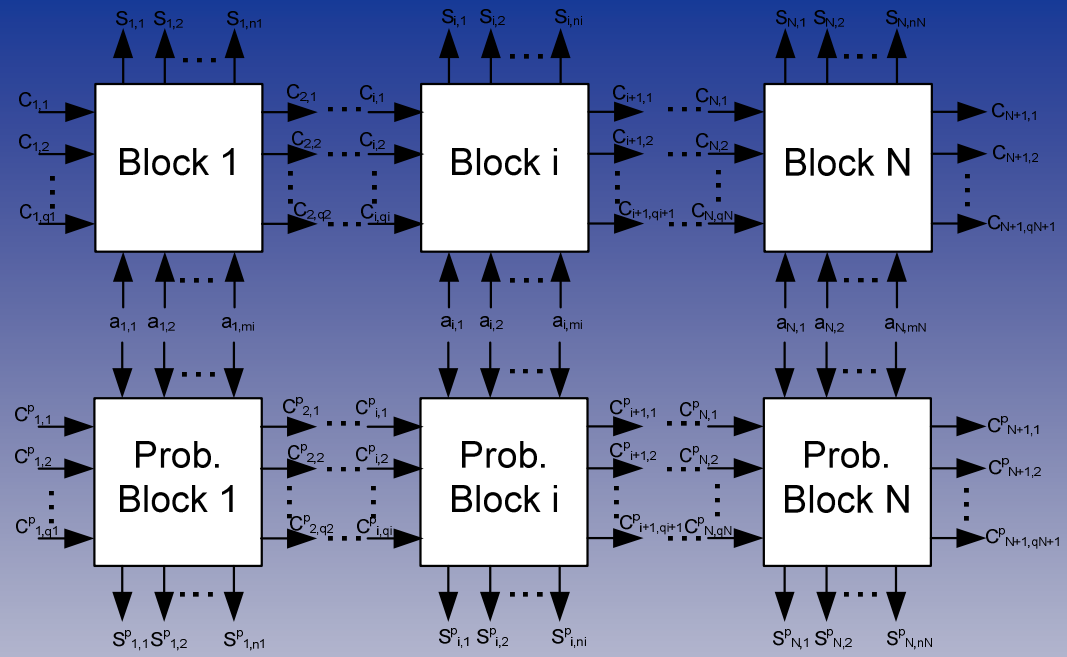
- Anshul Singh, Satyam Mandavilli, Vincent J. Mooney III and Keck-Voon Ling, "**A novel and fast method for characterizing noise based PCMOS circuits**," ASQED 2011, Kuala Lumpur, Malaysia.
- Anshul Singh, Arindam Basu, Keck-Voon Ling and Vincent J. Mooney III, "**Modeling multi-output filtering effects in PCMOS**," VLSI-DAT, April 25-27, Hsinchu, Taiwan, pp. 414-417, 2011.
- Arun Bhanu, Mark S. K. Lau, Keck-Voon Ling, Vincent J. Mooney III and Anshul Singh, "**A more precise model of noise based PCMOS errors**," Proceedings of DELTA, pp. 99-102, 2010.

asQED Symposium 2011

Error-Rate Prediction: The Cascade Math Model

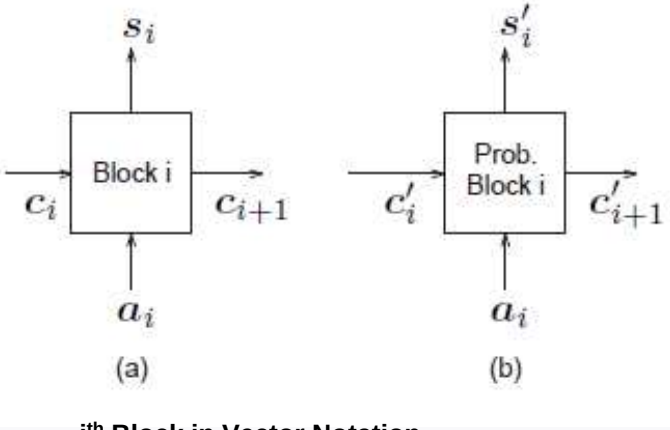
- Lau et al. have come up with a methodology to quickly predict the error-rates of cascade structure of blocks*.
- The methodology is based on
  - Knowing each block's output error-rate
  - Evaluation of mathematical equations that model the dynamics of error generation and propagation across the blocks.

*M. Lau, K. V. Ling, A. Bhanu, and V. J. Mooney III, "Error Rate Prediction for Probabilistic Circuits with More General Structures", The 16th Workshop on Synthesis And System Integration of Mixed Information technologies" (SASIMI2010), 18-19 October, 2010, Taipei, Taiwan, pp.220-225



Cascade Structure of Blocks

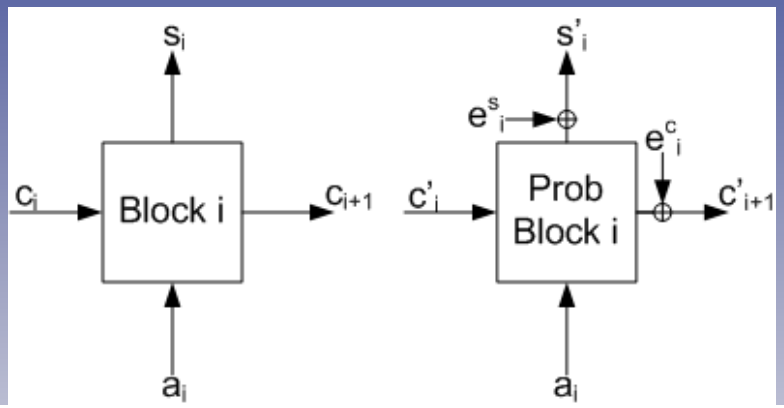
Terminology	Symbols for the ith block
Addend	$a_i = (a_{i,1}, a_{i,2}, \ldots, a_{i,m_i})$
Carry-in	$c_i = (c_{i,1}, c_{i,2}, \ldots, c_{i,q_i})$
Carry-out	$c_{i+1} = (c_{i+1,1}, \ldots, c_{i+1,q_{i+1}})$
Probabilistic carry-in	$c'_i = (c'_{i,1}, c'_{i,2}, \ldots, c'_{i,q_i})$
Probabilistic carry-out	$c'_{i+1} = (c'_{i+1,1}, \ldots, c'_{i+1,q_{i+1}})$
Carry-out bit-flip indicator	$e^c_i = (e^c_{i,1}, e^c_{i,2}, \ldots, e^c_{i,q_{i+1}})$
Sum	$s_i = (s_{i,1}, s_{i,2}, \ldots, s_{i,n_i})$
Probabilistic sum	$s'_i = (s'_{i,1}, s'_{i,2}, \ldots, s'_{i,n_i})$
Sum bit-flip indicator	$e^s_i = (e^s_{i,1}, e^s_{i,2}, \ldots, e^s_{i,n_i})$



i^{th} Block in Vector Notation

asQED Symposium 2011

The Cascade Math Model: Equations



$$P(c'_{i+1}=\alpha, c_{i+1}=\beta) = \sum_{\Omega} P(e^c_i=\gamma^c, c_i=\delta, c'_i=\epsilon, a_i=\zeta)$$

$$= \sum_{\Omega} P(e^c_i=\gamma^c \mid c_i=\delta, c'_i=\epsilon, a_i=\zeta) P(a_i=\zeta \mid c_i=\delta, c'_i=\epsilon) P(c_i=\delta, c'_i=\epsilon)$$

$$= \sum_{\Omega} P(e^c_i=\gamma^c \mid c'_i=\epsilon, a_i=\zeta) P(a_i=\zeta) P(c_i=\delta, c'_i=\epsilon).$$

$$P(s'_{ij} \neq s_{ij}) = \sum_{\Omega} P(e^s_{ij}=\gamma^s, c_i=\delta, c'_i=\epsilon, a_i=\zeta)$$

$$= \sum_{\Omega} P(e^s_{ij}=\gamma^s \mid c_i=\delta, c'_i=\epsilon, a_i=\zeta) P(a_i=\zeta \mid c_i=\delta, c'_i=\epsilon) P(c_i=\delta, c'_i=\epsilon)$$

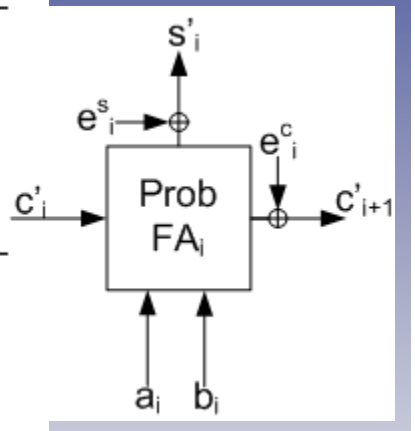
$$= \sum_{\Omega} P(e^s_{ij}=\gamma^s \mid c'_i=\epsilon, a_i=\zeta) P(a_i=\zeta) P(c_i=\delta, c'_i=\epsilon).$$

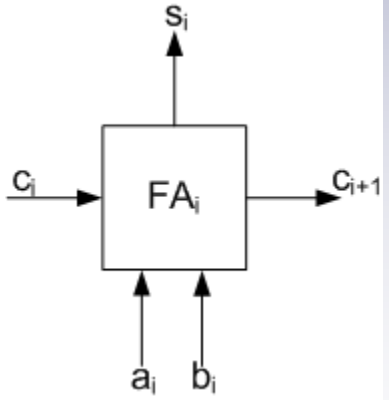
asQED Symposium 2011

Example - RCA

c_{i+1}	c'_{i+1}	c_i	c'_i	a_i	b_i	e^c_i
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	1	0	0	0
0	0	0	1	0	1	1
0	0	0	1	1	0	1
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	1
0	1	0	0	0	1	1
0	1	0	0	1	0	1
0	1	0	1	0	0	1
0	1	0	1	0	1	0
0	1	0	1	1	0	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	1	1
1	0	0	1	1	1	1
1	0	1	0	0	1	0
1	0	1	0	1	0	0
1	0	1	0	1	1	1
1	0	1	1	0	1	1
1	0	1	1	1	0	1
1	0	1	1	1	1	1
1	1	0	0	1	1	0
1	1	0	1	1	1	0
1	1	1	0	0	1	1
1	1	1	0	1	0	1
1	1	1	0	1	1	0
1	1	1	1	0	1	0
1	1	1	1	1	0	0
1	1	1	1	1	1	0

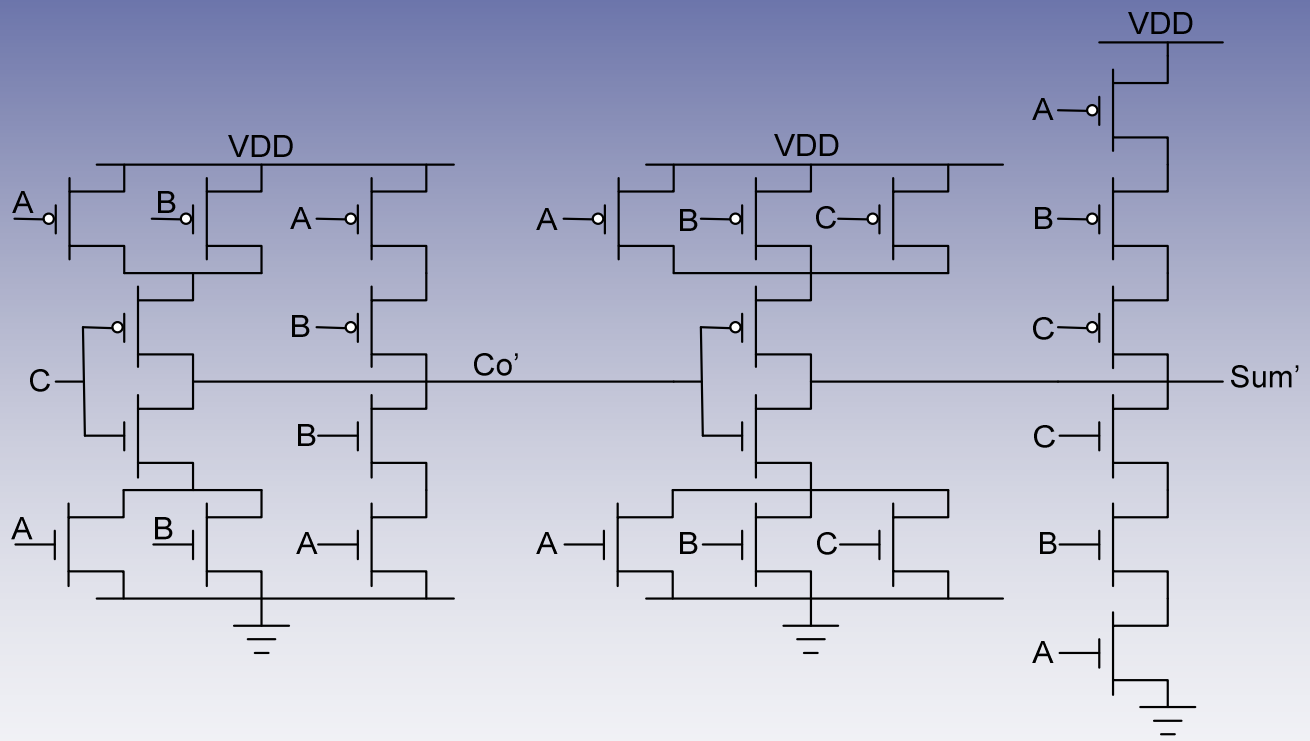
s_i	s'_i	c_i	c'_i	a_i	b_i	e^s_i
0	0	0	0	0	0	0
0	0	0	0	1	1	0
0	0	0	1	0	0	1
0	0	0	1	1	1	1
0	0	1	0	0	1	1
0	0	1	0	1	0	1
0	0	1	1	0	1	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	0	1	1	1
0	1	0	1	0	0	0
0	1	0	1	1	1	0
0	1	1	0	0	1	0
0	1	1	0	1	0	0
0	1	1	1	0	1	1
0	1	1	1	1	0	1
1	0	0	0	0	1	1
1	0	0	0	1	0	1
1	0	0	1	0	1	0
1	0	0	1	1	0	0
1	0	1	0	0	0	0
1	0	1	0	1	1	0
1	0	1	1	0	0	1
1	0	1	1	1	1	1
1	1	0	0	0	1	0
1	1	0	0	1	0	0
1	1	0	1	0	1	1
1	1	0	1	1	0	1
1	1	1	0	0	0	1
1	1	1	0	1	1	1
1	1	1	1	0	0	0
1	1	1	1	1	1	0





asQED Symposium 2011

Full Adder



Transistor level diagram of FA