Golay and Wavelet Error Control Codes in VLSI

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Introduction

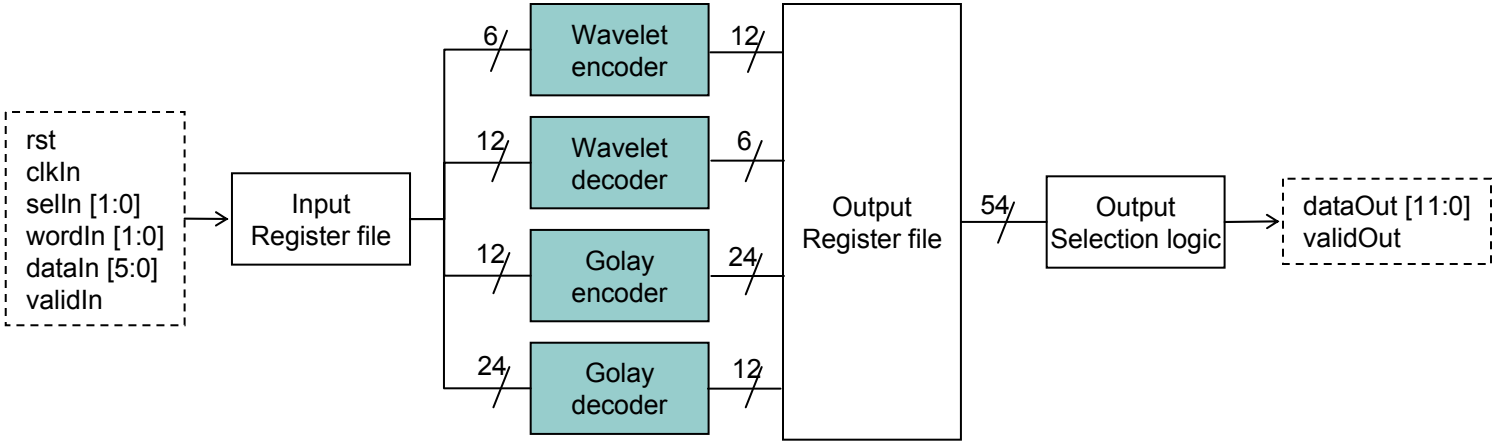
- First-ever VLSI implementation of wavelet and wavelet-based golay error control codes [1, 2]
- Wavelet code (12, 6, 4)* corrects 1-bit errors
- Wavelet-based golay (24, 12, 8)* corrects up to 3-bit errors

*(N, M, d) : (N=code length, M=message length, d=distance)

[1] F. Fekri, S. W. Mclaughlin, R. M. Mersereau and R. W. Schafer, "*Double circulant self-dual codes using finite field wavelet transforms," Springer Verlag Lecture Notes in Computer Science* (LNCS); Applied Algebra, Algebraic algorithms and Error-Correcting Codes, pp355-364, 1999.

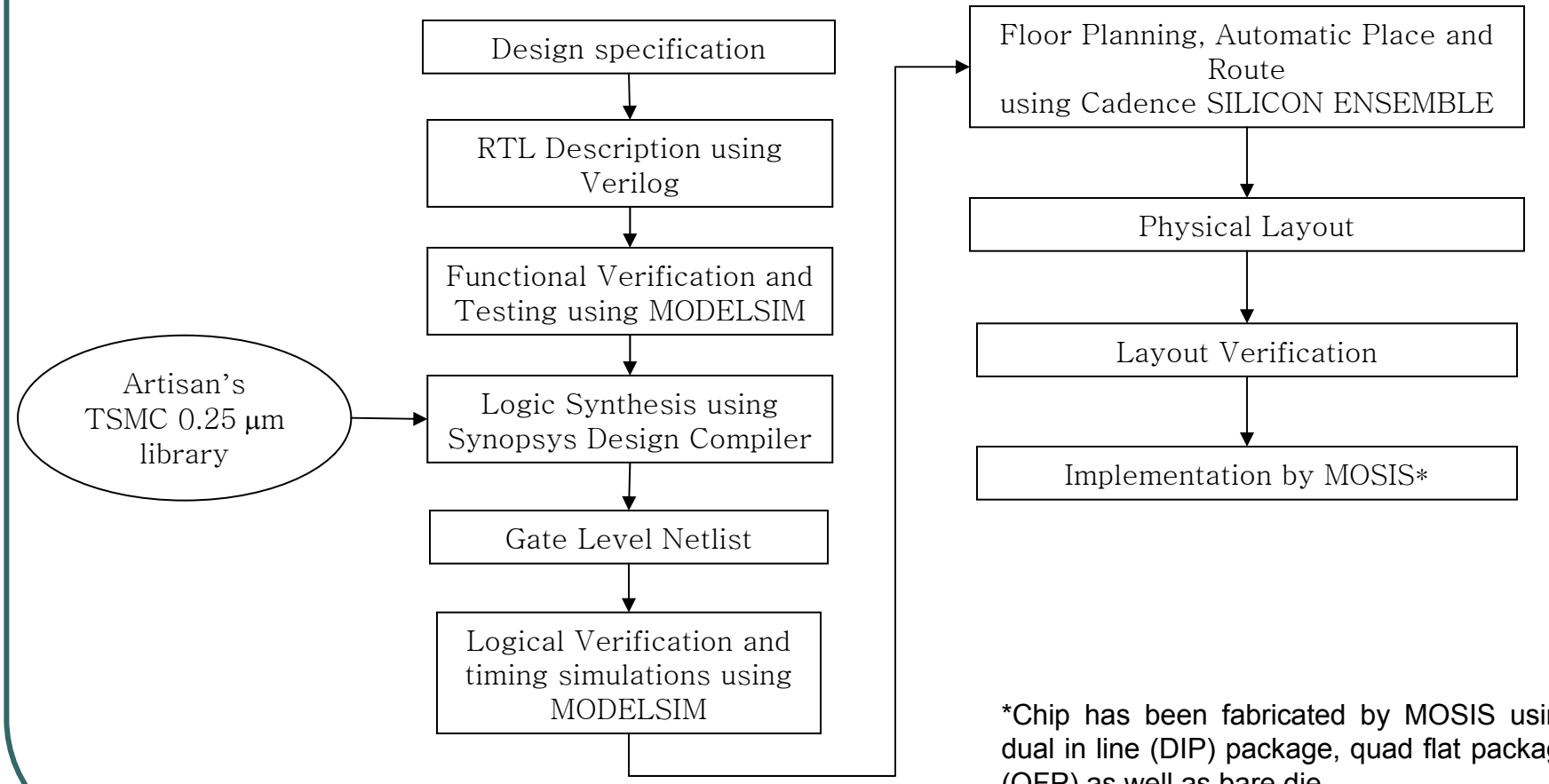
[2] F. Fekri, S. W. Mclaughlin, R. M. Mersereau and R. W. Schafer, "Decoding of half-rate wavelet codes; golay code and more," *Proceedings of IEEE International Conference on Acoustics, Speech, and Signal Processing* (ICASSP '01), Vol. 4, pp. 2609-2612, 2001.

Architecture



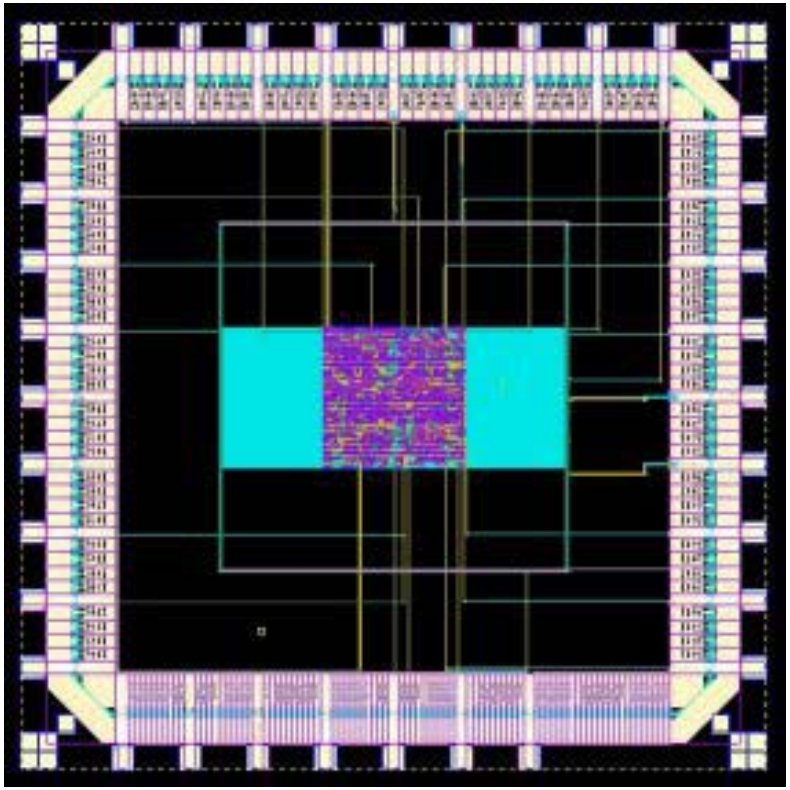
- RTL descriptions of the circuit designed in Verilog
- Four encoding and decoding modules (*selIn* signal chooses one of encoding/decoding modules)
- The width of Input and output is optimized for the wavelet encoder (i.e., 6-bit input and 12-bit output)
- 12- and 24-bit input requires 2 and 4 cycles, respectively; 24-bit output requires 2 cycles
- Encoding/decoding functions are implemented largely in combinational *XOR* logic
- Wavelet encoding/decoding and golay encoding are implemented in single stage combinational block
- Golay decoder uses a sequential logic block with a latency of 12 cycles

Design Flow

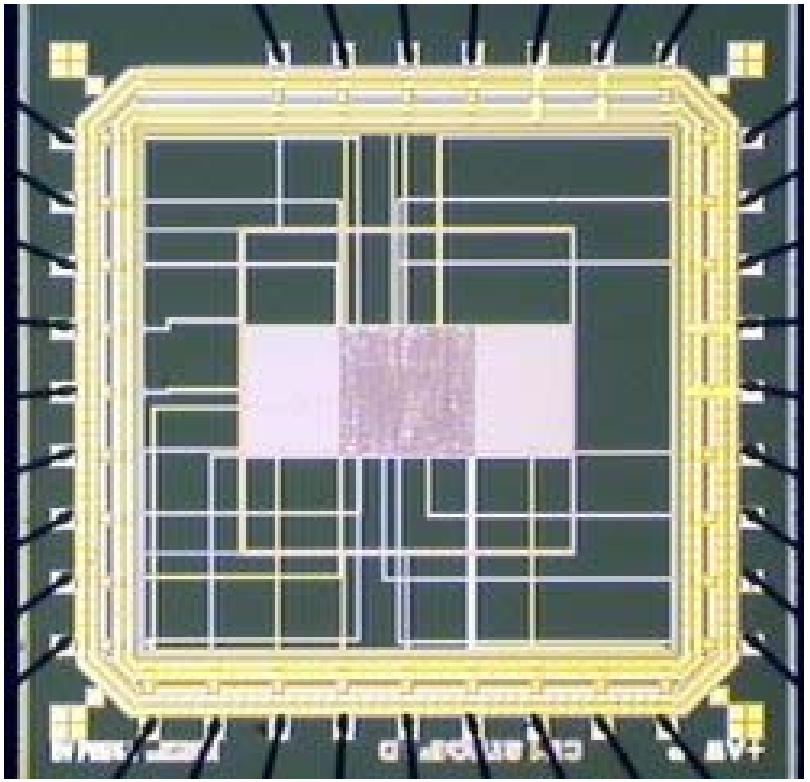


*Chip has been fabricated by MOSIS using dual in line (DIP) package, quad flat package (QFP) as well as bare die

Layout

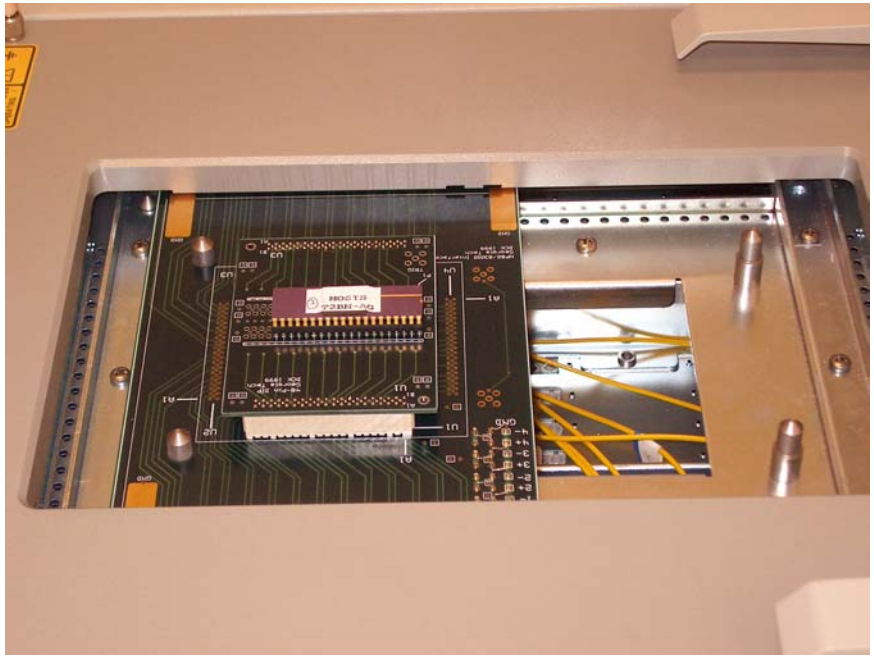


Physical layout prior to fabrication
Silicon size: 2637 x 2640 microns=6.9mm^2
(as given by MOSIS)



Chip layout with wire connections to the DIP after fabrication (taken at Georgia Tech)

Testing & Result



- Tested using HP 83000 Digital IC Test system
- The encoder/decoder logic has been successfully tested for its functionality
- A clock period of 6.9 ns (a speed of 145 MHz) achieved
- The effective data throughput is 145Mhz x 6bits=870Mb/sec.