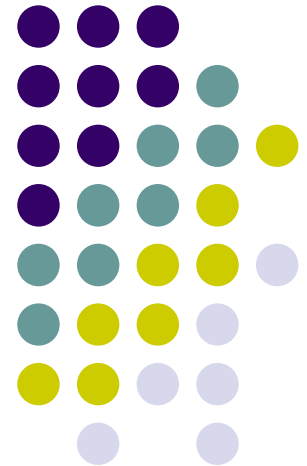


# Sleepy Stack Reduction of Leakage Power

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*Center for Research on Embedded Systems and Technology  
School of Electrical and Computer Engineering  
Georgia Institute of Technology, Atlanta, Georgia, U.S.A.*

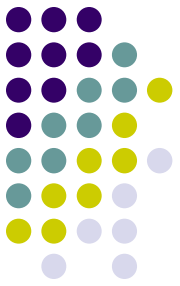


# Sleepy Stack Introduction



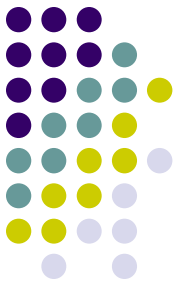
- **State-Saving Static Power Approach**
- **Tradeoffs**
  - Ultra-low static power
  - Area, delay penalties
- **Subthreshold leakage**
  - Source gating
  - High Threshold Voltage Transistors
  - Stack effect

# Previous Approaches

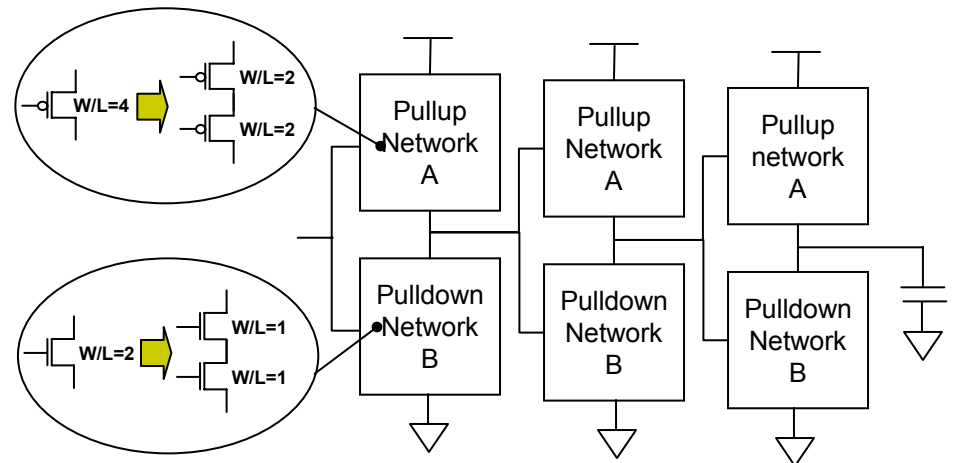


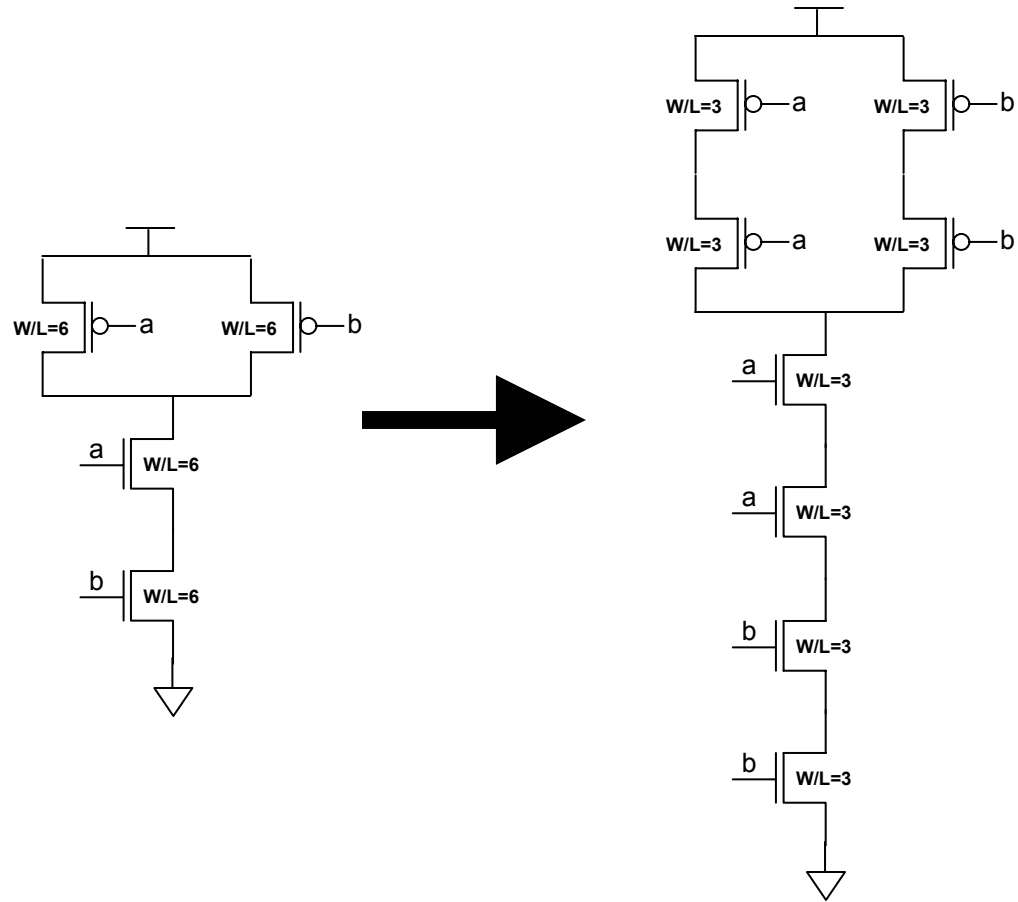
- **Stack**
  - Induce a reverse bias in cutoff
- **Sleep**
  - Disconnect Vdd/Gnd when circuit is idle
- **ZigZag**
  - Induce favorable state when circuit is idle
  - Disconnect one supply network terminal

# Stack Implementation



- Duplicate transistors
  - Forces negative  $V_{gs}$  in cut-off
- Delay Penalty
  - Sizing tradeoff: greater gate capacitance or greater resistance?
  - Half-width transistors
- Dual  $V_{th}$  applicability
  - 4x delay increase

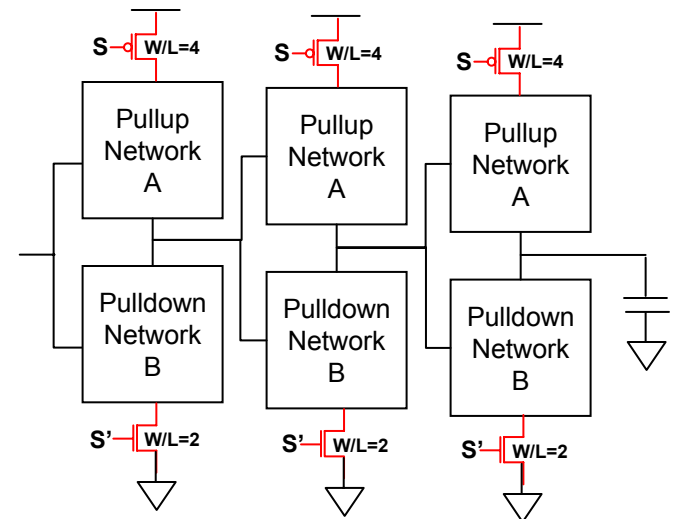




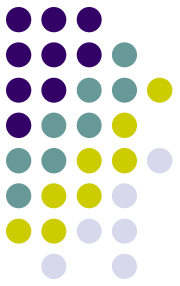
# Sleep Implementation



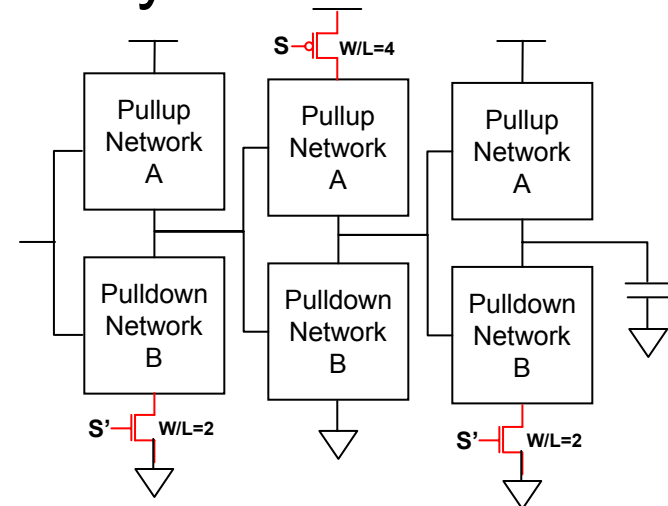
- Source Gating
- Dual threshold possibility
  - Sleep transistors can be slow
- Additional routing
  - S and complement
  - “Virtual” Vdd / Gnd
- State Destructive
- Floating Output



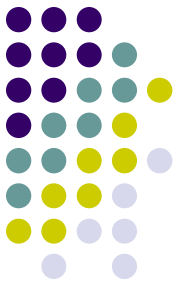
# ZigZag Implementation



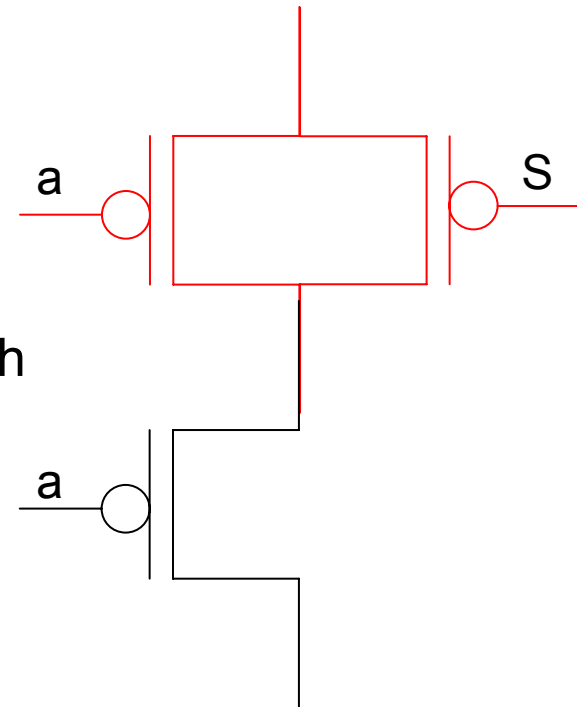
- Favored input vector
- Faster recovery than sleep approach
  - An optimal input vector is pre-loaded
  - No recovery from Z necessary
- State destructive
- High  $V_{th}$  applicable



# Sleepy Stack

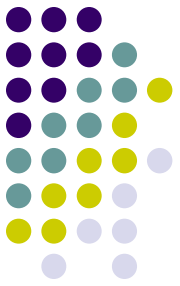


- Sleepy stack
  - Source gating
  - Stack effect
- Novel application of dual  $V_{th}$ 
  - Decreased delay penalty
  - Effective leakage reduction





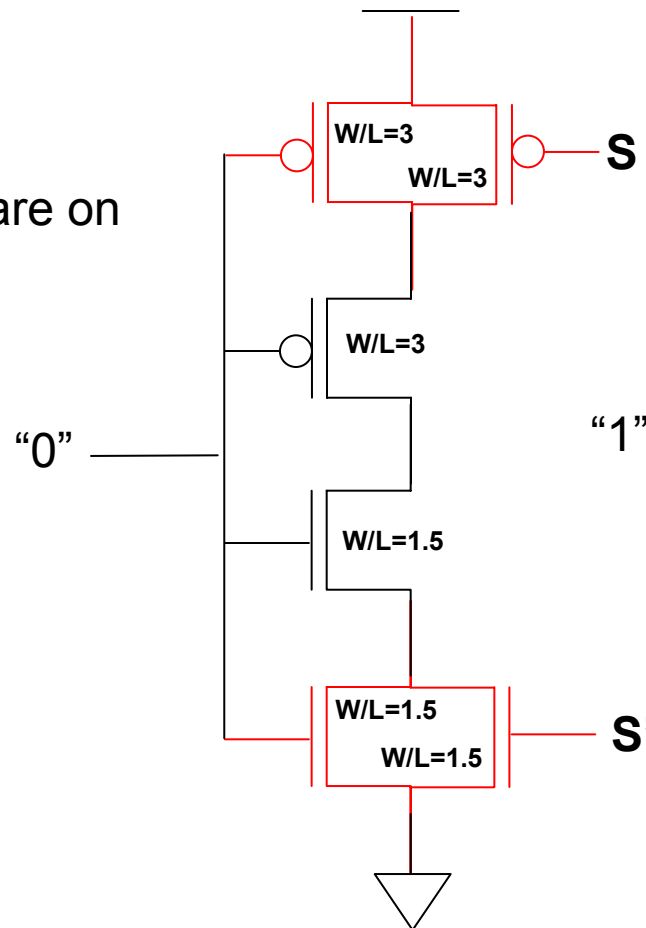
# Inverter, input “0”



## Normal Operation:

$$S = 0, S' = 1$$

High  $V_{th}$  transistors are on



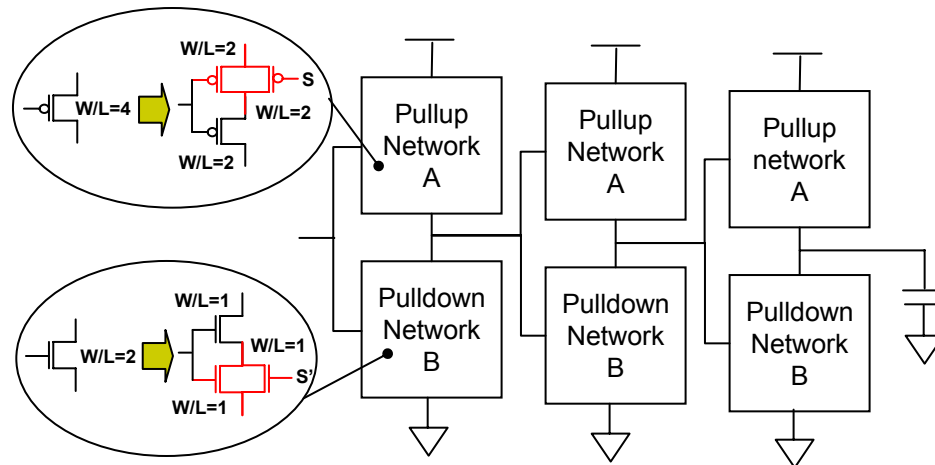
## Power Saving

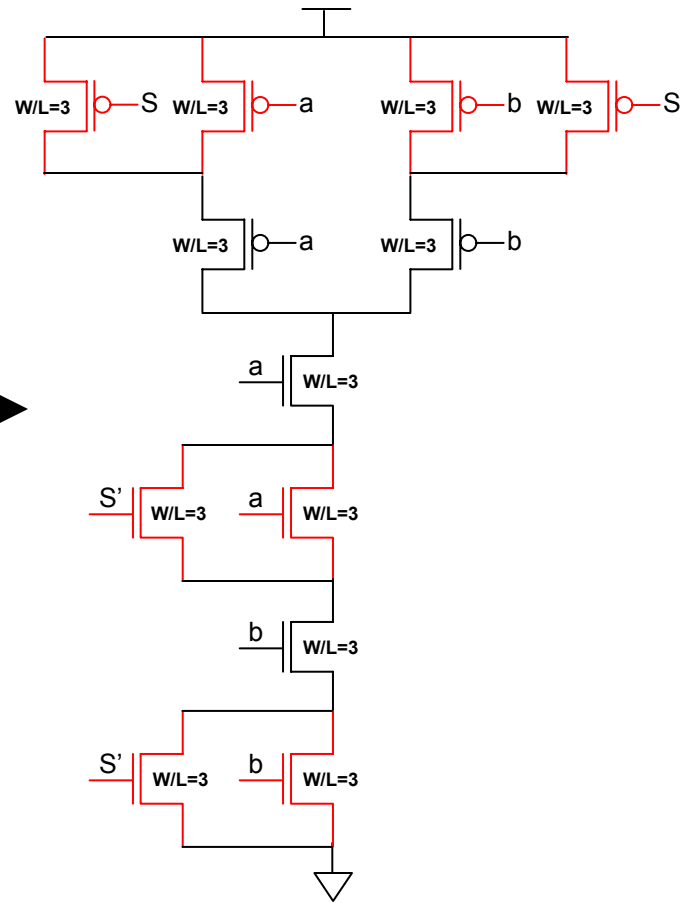
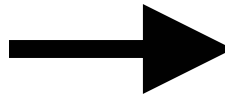
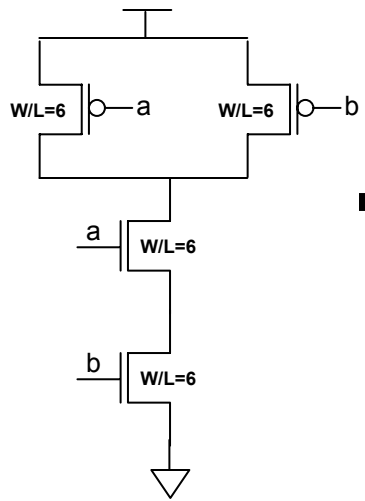
$$S = 1, S' = 0$$

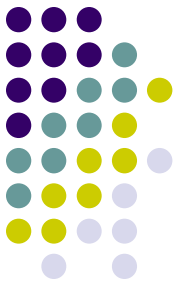
# Sleepy Stack



- State-saving
  - Path to Vdd/Gnd
  - Effective blocking of complement
- Use of high  $V_{th}$  only to block leakage current







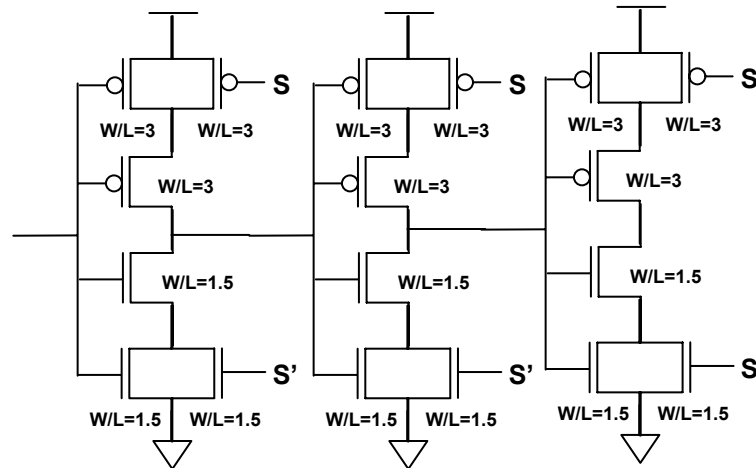
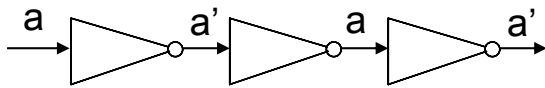
# Assessments

- Implementations
  - 3 Inverter chain
  - 4:1 MUX
  - Full adder
- Criteria
  - Static Power
  - Dynamic Power
  - Delay
  - Area

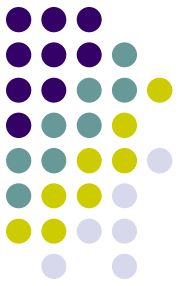
# Implementations



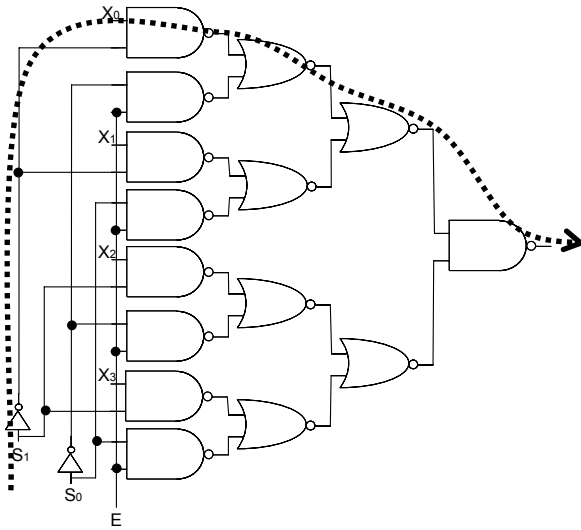
## 3 Inverter Chain



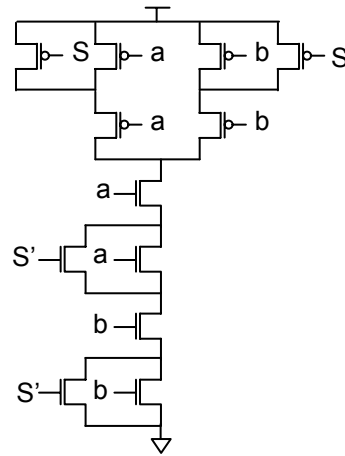
# Implementations



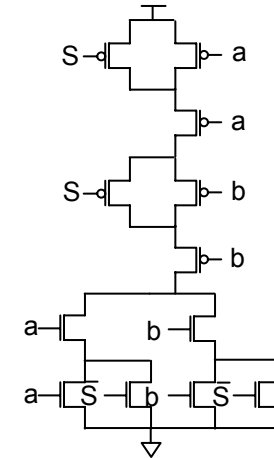
## 4:1 MUX



4:1 MUX

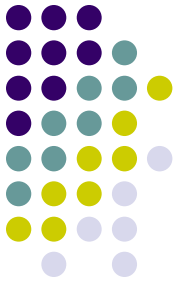


NAND

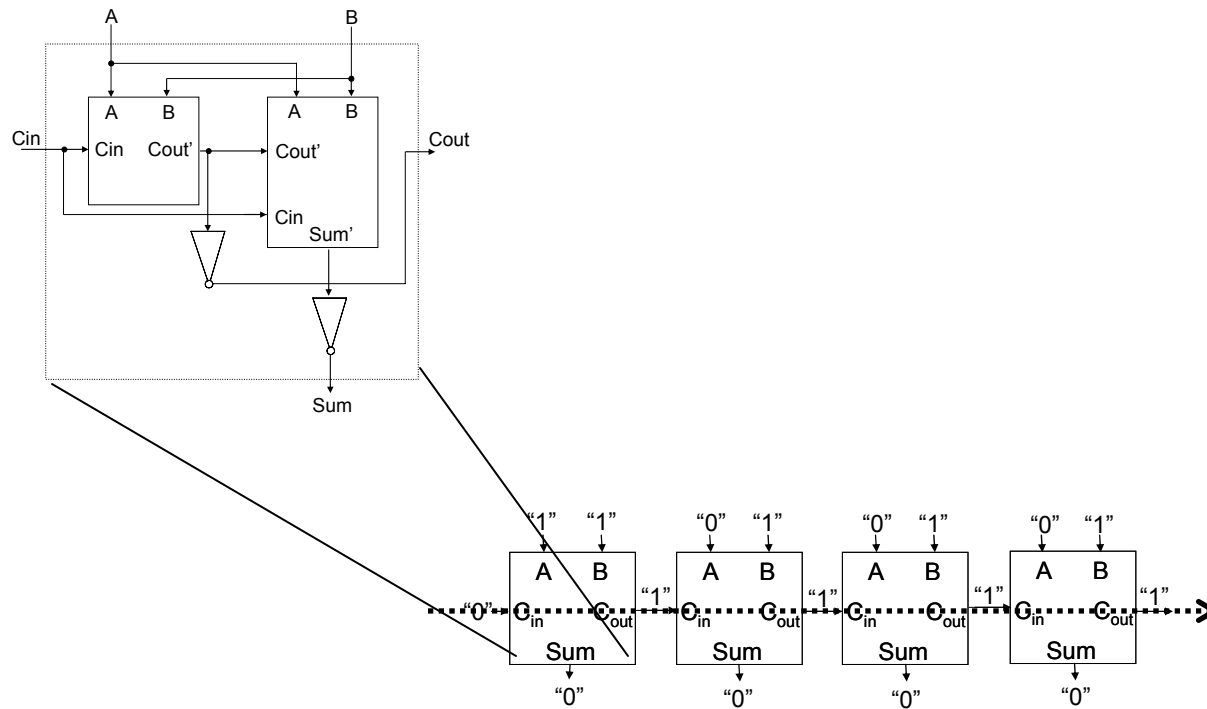


NOR

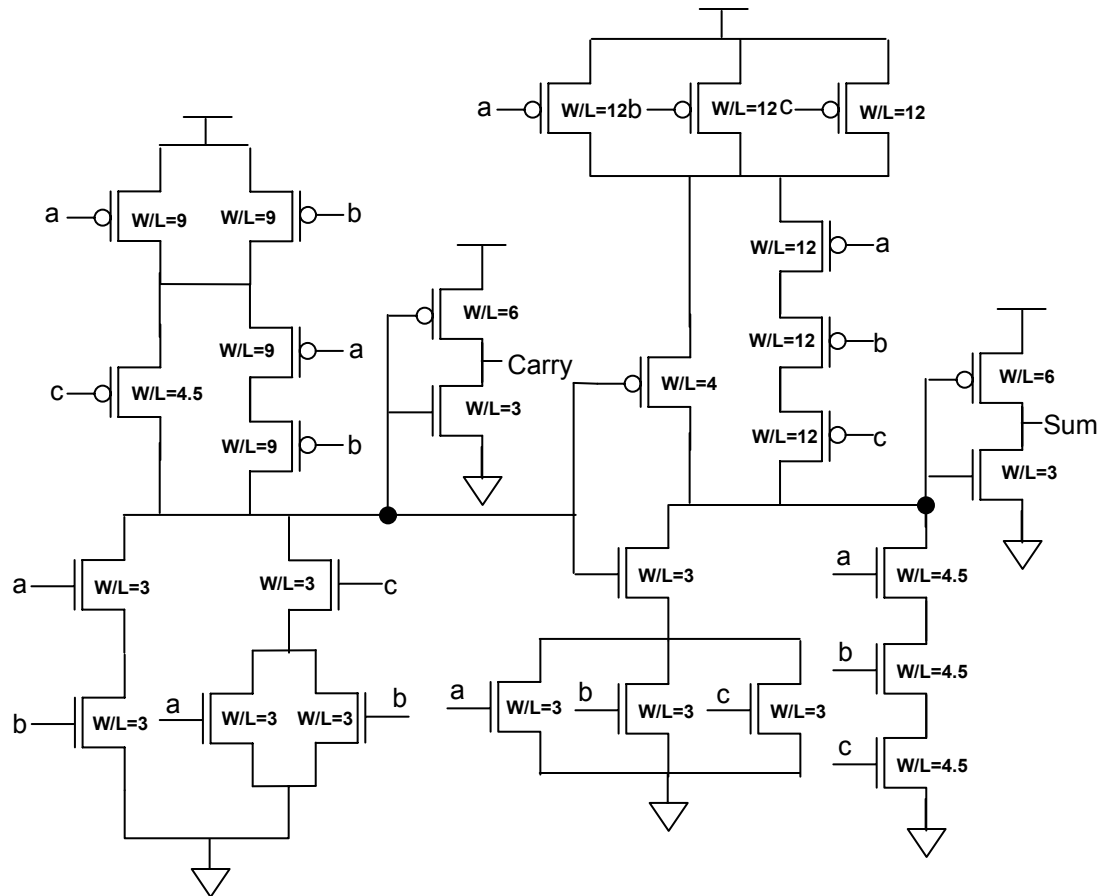
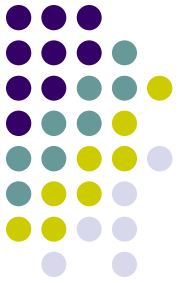
# Implementations



## 4 Adder Chain

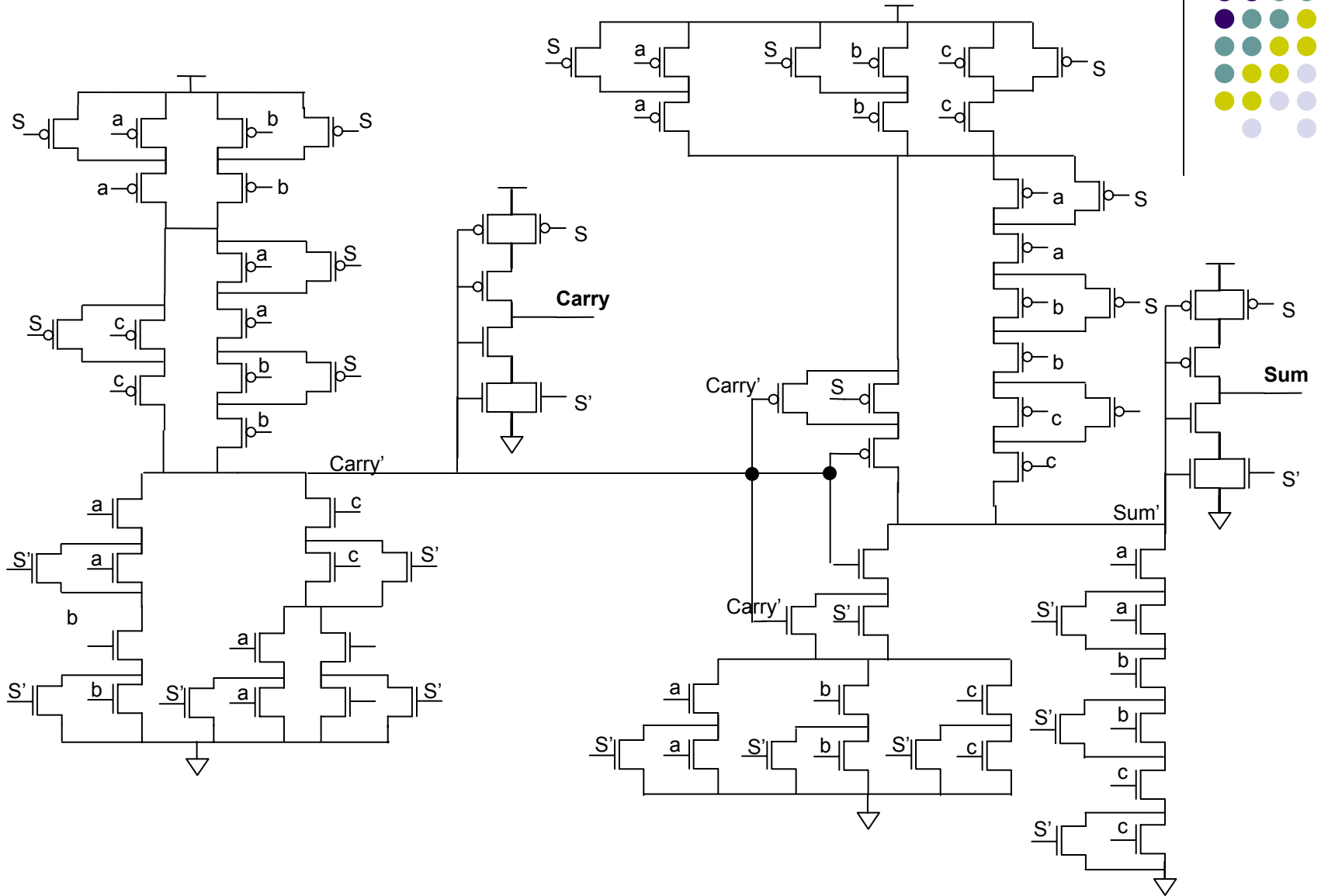
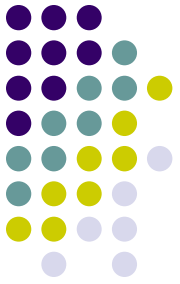


# Full Adder (Base Case)





# Full Adder (Sleepy Stack)



# Experiments



- Simulation-based measurements
  - Avant! HSPICE <sup>[11]</sup>
  - NCSU Model targeting TSMC's process for 0.18u
  - Berkeley Model for 0.18u, 0.13u, 0.10u, 0.07u <sup>[12]</sup>
- Criteria
  - Delay across critical path
  - Average dynamic and static power
  - Area
    - Cadence Virtuoso
    - Full layouts for TSMC 0.18u
    - Scaled for 0.13u, 0.10u, 0.07u

# 3 Inverter Chain

TSMC 0.18 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	9.56E-11	4.50E-11	3.16E-06	23.59
Stack	2.46E-10	8.99E-12	3.20E-06	26.91
Sleep	1.56E-10	1.44E-11	4.79E-06	48.09
ZigZag	1.34E-10	5.63E-12	5.43E-06	33.32
Sleepy Stack	1.78E-10	1.64E-11	3.46E-06	40.73
Sleep (dual Vth)	2.22E-10	1.09E-12	4.56E-06	48.09
ZigZag (dual Vth)	1.76E-10	1.06E-17	5.21E-06	33.32
Sleepy Stack (dual Vth)	2.19E-10	5.96E-16	3.18E-06	40.73

Berkeley 0.18 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	7.73E-11	1.70E-09	4.94E-06	23.59
Stack	1.95E-10	2.31E-10	3.63E-06	26.91
Sleep	1.06E-10	5.48E-10	7.79E-06	48.09
ZigZag	1.01E-10	3.31E-10	8.69E-06	33.32
Sleepy Stack	1.38E-10	4.05E-10	4.85E-06	40.73
Sleep (dual Vth)	1.55E-10	1.11E-12	6.83E-06	48.09
ZigZag (dual Vth)	1.47E-10	4.14E-16	8.04E-06	33.32
Sleepy Stack (dual Vth)	1.87E-10	4.99E-14	3.99E-06	40.73

Berkeley 0.13 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	7.00E-11	1.48E-09	2.15E-06	13.54
Stack	1.70E-10	1.00E-10	1.56E-06	15.44
Sleep	9.34E-11	2.64E-10	3.21E-06	27.59
ZigZag	8.14E-11	2.32E-10	4.03E-06	19.12
Sleepy Stack	1.20E-10	1.82E-10	2.03E-06	23.37
Sleep (dual Vth)	1.41E-10	6.73E-13	2.62E-06	27.59
ZigZag (dual Vth)	1.07E-10	8.92E-15	3.50E-06	19.12
Sleepy Stack (dual Vth)	1.64E-10	1.75E-13	1.77E-06	23.37

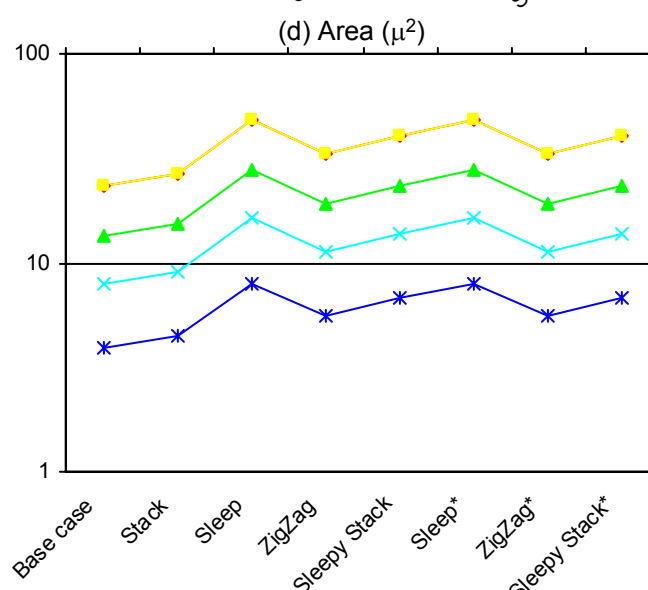
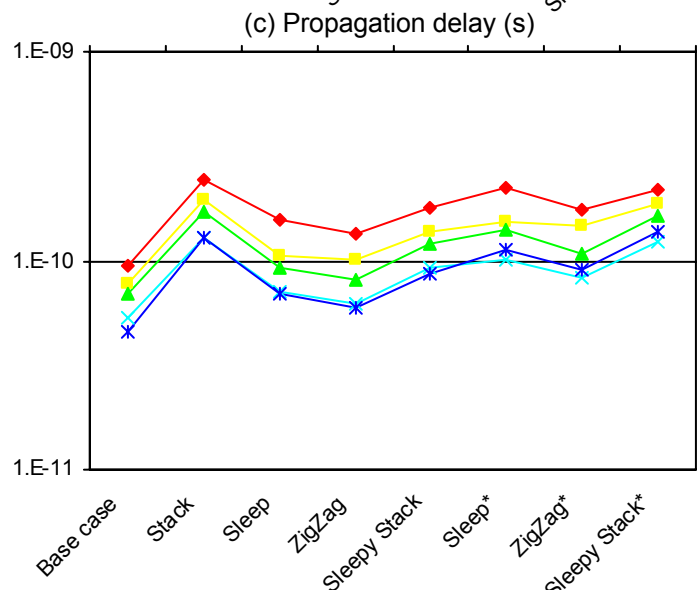
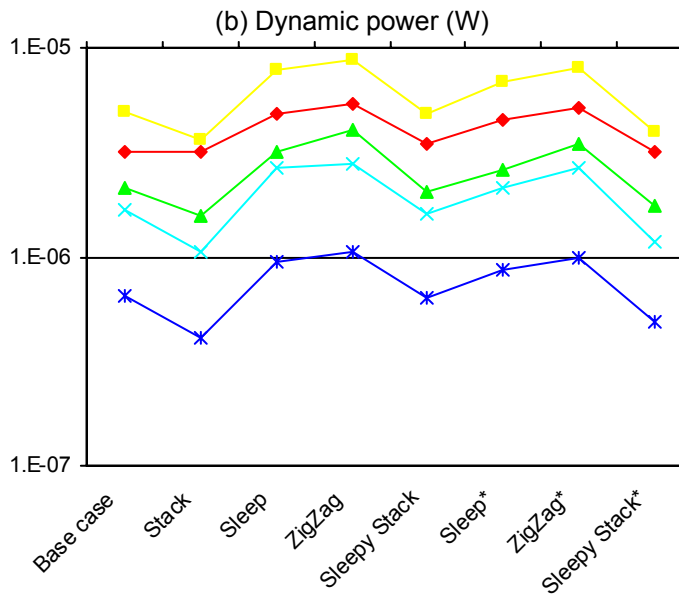
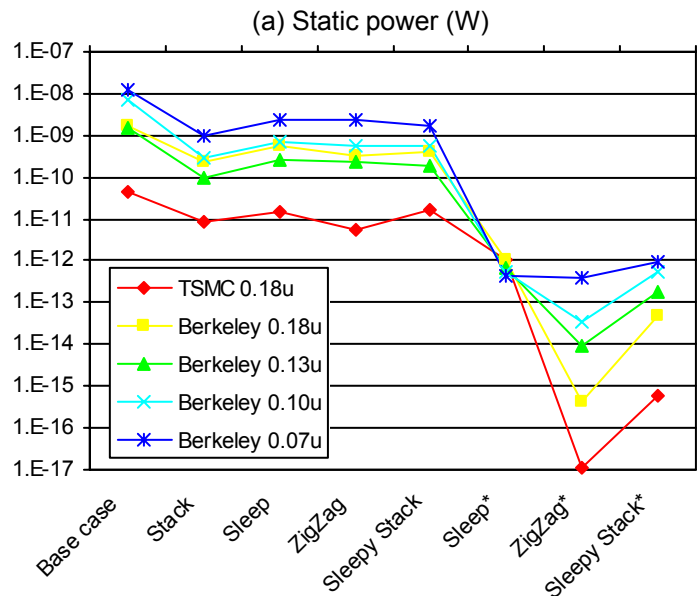
Berkeley 0.10 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	5.36E-11	6.74E-09	1.67E-06	8.01
Stack	1.30E-10	2.87E-10	1.05E-06	9.14
Sleep	7.05E-11	6.77E-10	2.66E-06	16.33
ZigZag	6.21E-11	5.40E-10	2.80E-06	11.31
Sleepy Stack	9.28E-11	5.39E-10	1.60E-06	13.83
Sleep (dual Vth)	1.02E-10	5.39E-13	2.15E-06	16.33
ZigZag (dual Vth)	8.28E-11	3.44E-14	2.68E-06	11.31
Sleepy Stack (dual Vth)	1.22E-10	5.18E-13	1.17E-06	13.83

Berkeley 0.07 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	4.61E-11	1.24E-08	6.56E-07	3.92
Stack	1.28E-10	9.89E-10	4.08E-07	4.48
Sleep	6.98E-11	2.40E-09	9.49E-07	8.00
ZigZag	5.99E-11	2.27E-09	1.05E-06	5.54
Sleepy Stack	8.75E-11	1.77E-09	6.35E-07	6.78
Sleep (dual Vth)	1.14E-10	4.32E-13	8.58E-07	8.00
ZigZag (dual Vth)	9.03E-11	3.84E-13	9.87E-07	5.54
Sleepy Stack (dual Vth)	1.38E-10	9.88E-13	4.88E-07	6.78

# 3-inv highlights of state saving approaches

- Static Power
  - Stack approach (single  $V_{th}$ )
    - 0.18u: 2.31E-10
    - 0.07u: 9.89E-10
  - Sleepy Stack approach (dual  $V_{th}$ )
    - 0.18u: 4.99E-14 (**4629x reduction**)
    - 0.07u: 9.88E-13 (**1001x reduction**)
- Delay
  - Stack approach (single  $V_{th}$ )
    - 0.18u: 1.95E-10 s
    - 0.07u: 1.28E-10 s
  - Sleepy Stack approach (dual  $V_{th}$ )
    - 0.18u: 1.87E-10 s (**4% faster**)
    - 0.07u: 1.38E-10 s (**7% slower**)
- Area
  - Sleepy Stack approach requires 72% more area than the stack approach

# 3 Inverter Chain Results



# 4:1 MUX

TSMC 0.18 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	6.97E-10	3.87E-10	1.51E-04	138.00
Stack	1.70E-09	2.24E-10	1.30E-04	186.00
Sleep	9.43E-10	1.10E-10	1.55E-04	186.00
ZigZag	9.45E-10	5.49E-11	1.43E-04	166.00
Sleepy Stack	1.36E-09	1.58E-10	1.31E-04	396.00
Sleep (dual Vth)	1.26E-09	1.86E-11	1.59E-04	186.00
ZigZag (dual Vth)	1.26E-09	1.21E-11	1.43E-04	166.00
Sleepy Stack (dual Vth)	1.73E-09	3.83E-11	1.21E-04	396.00

Berkeley 0.18 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	5.07E-10	3.04E-08	1.41E-04	138.00
Stack	1.50E-09	2.96E-09	1.21E-04	186.00
Sleep	6.79E-10	4.51E-09	1.46E-04	186.00
ZigZag	6.83E-10	2.51E-09	1.35E-04	166.00
Sleepy Stack	1.18E-09	4.30E-09	1.27E-04	396.00
Sleep (dual Vth)	9.38E-10	1.33E-11	1.53E-04	186.00
ZigZag (dual Vth)	9.53E-10	8.12E-12	1.37E-04	166.00
Sleepy Stack (dual Vth)	1.63E-09	3.51E-11	1.18E-04	396.00

Berkeley 0.13 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	4.15E-10	2.40E-08	6.10E-05	79.18
Stack	1.21E-09	9.69E-10	5.20E-05	106.72
Sleep	5.46E-10	1.98E-09	6.19E-05	106.72
ZigZag	5.43E-10	1.25E-09	5.83E-05	95.25
Sleepy Stack	9.35E-10	1.63E-09	5.42E-05	227.21
Sleep (dual Vth)	7.53E-10	6.96E-12	6.47E-05	106.72
ZigZag (dual Vth)	7.56E-10	1.66E-12	5.90E-05	95.25
Sleepy Stack (dual Vth)	1.21E-09	2.22E-11	4.94E-05	227.21

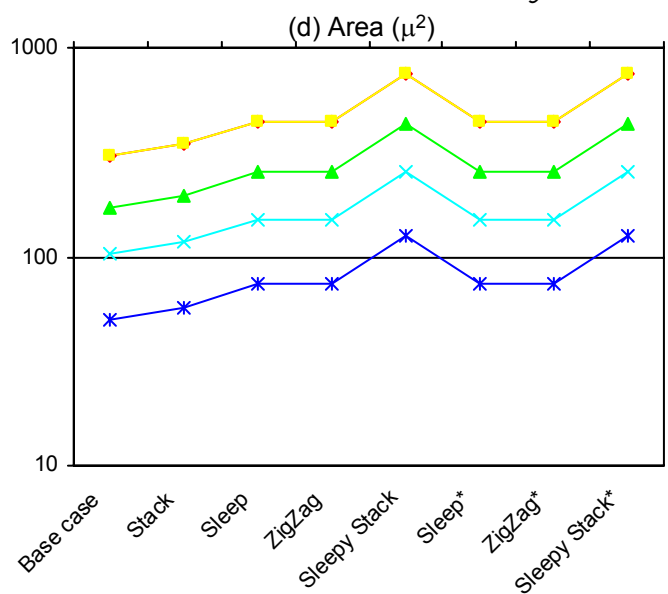
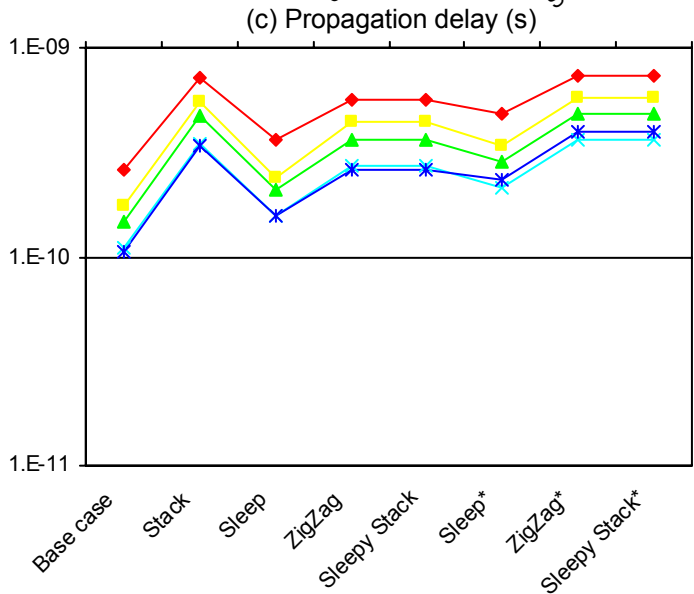
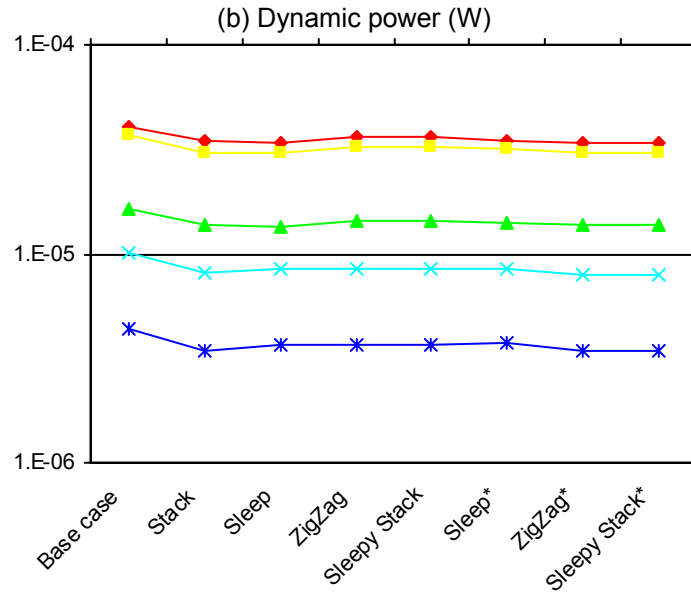
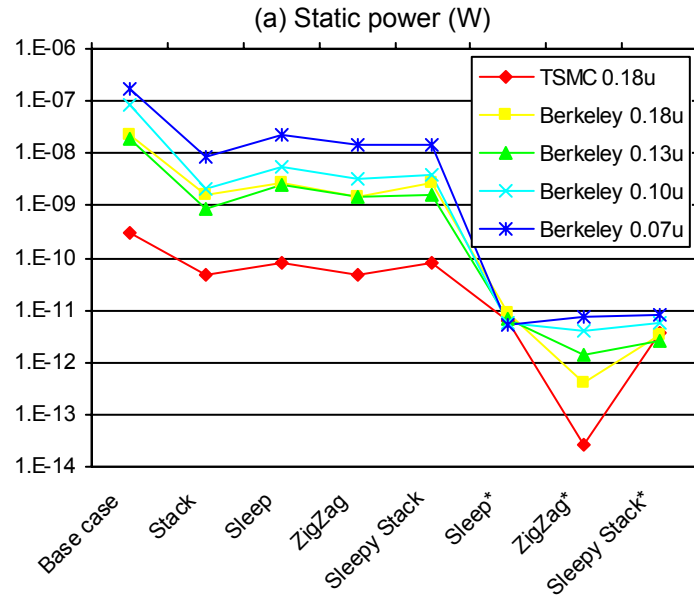
Berkeley 0.10 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	3.08E-10	9.75E-08	3.68E-05	46.85
Stack	8.95E-10	3.20E-09	3.00E-05	63.15
Sleep	4.13E-10	5.26E-09	3.73E-05	63.15
ZigZag	4.17E-10	3.23E-09	3.54E-05	56.36
Sleepy Stack	7.01E-10	5.05E-09	3.19E-05	134.44
Sleep (dual Vth)	5.55E-10	5.72E-12	3.85E-05	63.15
ZigZag (dual Vth)	5.62E-10	4.94E-12	3.55E-05	56.36
Sleepy Stack (dual Vth)	9.14E-10	2.38E-11	2.92E-05	134.44

Berkeley 0.07 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	2.91E-10	1.81E-07	1.52E-05	22.96
Stack	8.89E-10	9.25E-09	1.24E-05	30.94
Sleep	4.11E-10	1.69E-08	1.54E-05	30.94
ZigZag	4.06E-10	1.20E-08	1.47E-05	27.62
Sleepy Stack	6.79E-10	1.50E-08	1.31E-05	65.88
Sleep (dual Vth)	6.20E-10	3.31E-12	1.61E-05	30.94
ZigZag (dual Vth)	6.15E-10	4.92E-12	1.47E-05	27.62
Sleepy Stack (dual Vth)	1.03E-09	1.88E-11	1.22E-05	65.88

# 4:1 MUX highlights of state saving approaches

- Static Power
  - Stack approach (single  $V_{th}$ )
    - 0.18u: 1.55E-9
    - 0.07u: 8.63E-9
  - Sleepy Stack approach (dual  $V_{th}$ )
    - 0.18u: 3.42E-12 (**453x reduction**)
    - 0.07u: 8.19E-12 (**1053x reduction**)
- Delay
  - Stack approach (single  $V_{th}$ )
    - 0.18u: 5.50E-10 s
    - 0.07u: 3.39E-10 s
  - Sleepy Stack approach (dual  $V_{th}$ )
    - 0.18u: 5.76E-10 s (**5% slower**)
    - 0.07u: 3.97E-10 s (**15% slower**)
- Area
  - Sleepy Stack approach requires 118% more area than the stack approach

# 4:1 MUX Results





# Full Adder

TSMC 0.18 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	2.58E-10	2.89E-10	4.07E-05	301.60
Stack	7.26E-10	4.87E-11	3.45E-05	345.06
Sleep	3.63E-10	7.71E-11	3.40E-05	445.50
ZigZag	5.62E-10	4.75E-11	3.60E-05	447.00
Sleepy Stack	5.62E-10	8.31E-11	3.60E-05	753.40
Sleep (dual Vth)	4.87E-10	6.39E-12	3.47E-05	445.50
ZigZag (dual Vth)	7.41E-10	2.61E-14	3.37E-05	447.00
Sleepy Stack (dual Vth)	7.41E-10	3.67E-12	3.37E-05	753.40

Berkeley 0.18 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	1.77E-10	2.23E-08	3.69E-05	301.60
Stack	5.50E-10	1.55E-09	3.06E-05	345.06
Sleep	2.39E-10	2.81E-09	3.06E-05	445.50
ZigZag	4.38E-10	1.49E-09	3.27E-05	447.00
Sleepy Stack	4.38E-10	2.63E-09	3.27E-05	753.40
Sleep (dual Vth)	3.36E-10	8.69E-12	3.16E-05	445.50
ZigZag (dual Vth)	5.76E-10	3.98E-13	3.04E-05	447.00
Sleepy Stack (dual Vth)	5.76E-10	3.42E-12	3.04E-05	753.40

Berkeley 0.13 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	1.48E-10	1.84E-08	1.64E-05	173.05
Stack	4.71E-10	9.02E-10	1.38E-05	197.98
Sleep	2.07E-10	2.59E-09	1.36E-05	255.61
ZigZag	3.59E-10	1.48E-09	1.44E-05	256.47
Sleepy Stack	3.59E-10	1.58E-09	1.44E-05	432.27
Sleep (dual Vth)	2.87E-10	6.60E-12	1.40E-05	255.61
ZigZag (dual Vth)	4.86E-10	1.41E-12	1.37E-05	256.47
Sleepy Stack (dual Vth)	4.86E-10	2.61E-12	1.37E-05	432.27

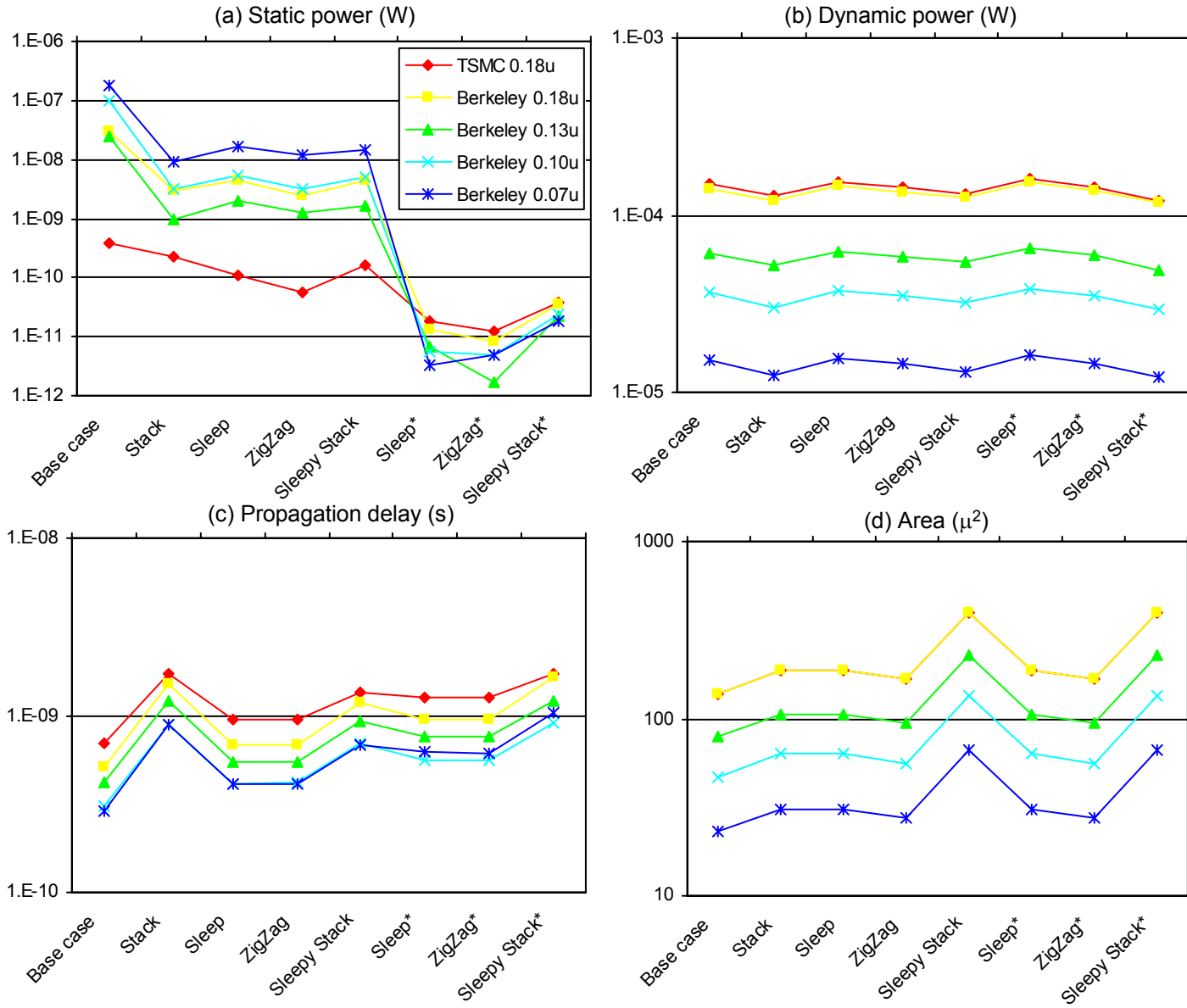
Berkeley 0.10 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	1.11E-10	8.62E-08	1.02E-05	102.40
Stack	3.51E-10	2.18E-09	8.03E-06	117.15
Sleep	1.57E-10	5.48E-09	8.39E-06	151.25
ZigZag	2.70E-10	3.16E-09	8.51E-06	151.76
Sleepy Stack	2.70E-10	3.97E-09	8.51E-06	255.78
Sleep (dual Vth)	2.12E-10	5.62E-12	8.50E-06	151.25
ZigZag (dual Vth)	3.59E-10	3.97E-12	7.95E-06	151.76
Sleepy Stack (dual Vth)	3.59E-10	5.46E-12	7.95E-06	255.78

Berkeley 0.07 $\mu$	Propagation delay (s)	Static Power (W)	Dynamic Power (W)	Area ( $\mu^2$ )
Base case	1.05E-10	1.72E-07	4.35E-06	50.17
Stack	3.39E-10	8.63E-09	3.43E-06	57.40
Sleep	1.56E-10	2.24E-08	3.66E-06	74.11
ZigZag	2.58E-10	1.41E-08	3.64E-06	74.36
Sleepy Stack	2.58E-10	1.51E-08	3.64E-06	125.33
Sleep (dual Vth)	2.35E-10	5.03E-12	3.73E-06	74.11
ZigZag (dual Vth)	3.97E-10	7.54E-12	3.43E-06	74.36
Sleepy Stack (dual Vth)	3.97E-10	8.19E-12	3.43E-06	125.33

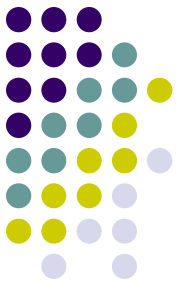
# Adder highlights of state saving approaches

- Static Power
  - Stack approach (single  $V_{th}$ )
    - 0.18u: 2.96E-9 W
    - 0.07u: 9.25E-9 W
  - Sleepy Stack approach (dual  $V_{th}$ )
    - 0.18u: 3.51E-11 W (**84x reduction**)
    - 0.07u: 1.88E-11 W (**492x reduction**)
- Delay
  - Stack approach (single  $V_{th}$ )
    - 0.18u: 1.50E-9s
    - 0.07u: 8.89E-10s
  - Sleepy Stack approach (dual  $V_{th}$ )
    - 0.18u: 1.63E-9s (**8% slower**)
    - 0.07u: 1.03E-9s (**14% slower**)
- Area
  - Sleepy Stack approach requires 147% more area than the stack approach

# Full Adder Results



# Conclusions



- Niche application
  - Ultra-low static power
    - Up to 1000x lower than stack approach
    - Roughly same delay
    - +/- 50% of sleep and zigzag approaches
  - High area
    - 72% - 118% increase over stack approach
  - Dual threshold processes
  - State saving
- Standard Cell library
  - Composite simple gates
  - Gates with 2 inputs optimal