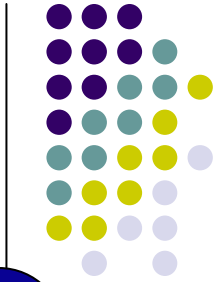


Automated Bus Generation for Multiprocessor SoC Design

Kyeong Keol Ryu and Vincent J. Mooney III
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA, USA

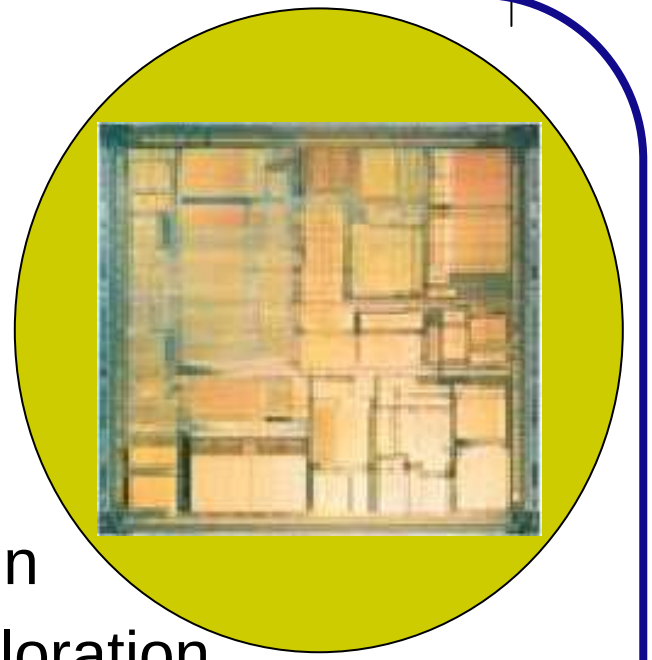
March 5, 2003

Outline

- Introduction
- Related Work
- Bus System Structure
- Bus Generation Tool and It's User Options
- Bus Generation Sequence with an Example: BFBA
- Application Examples
- Experimental Environment
- Performance Evaluation
- Conclusion

Introduction

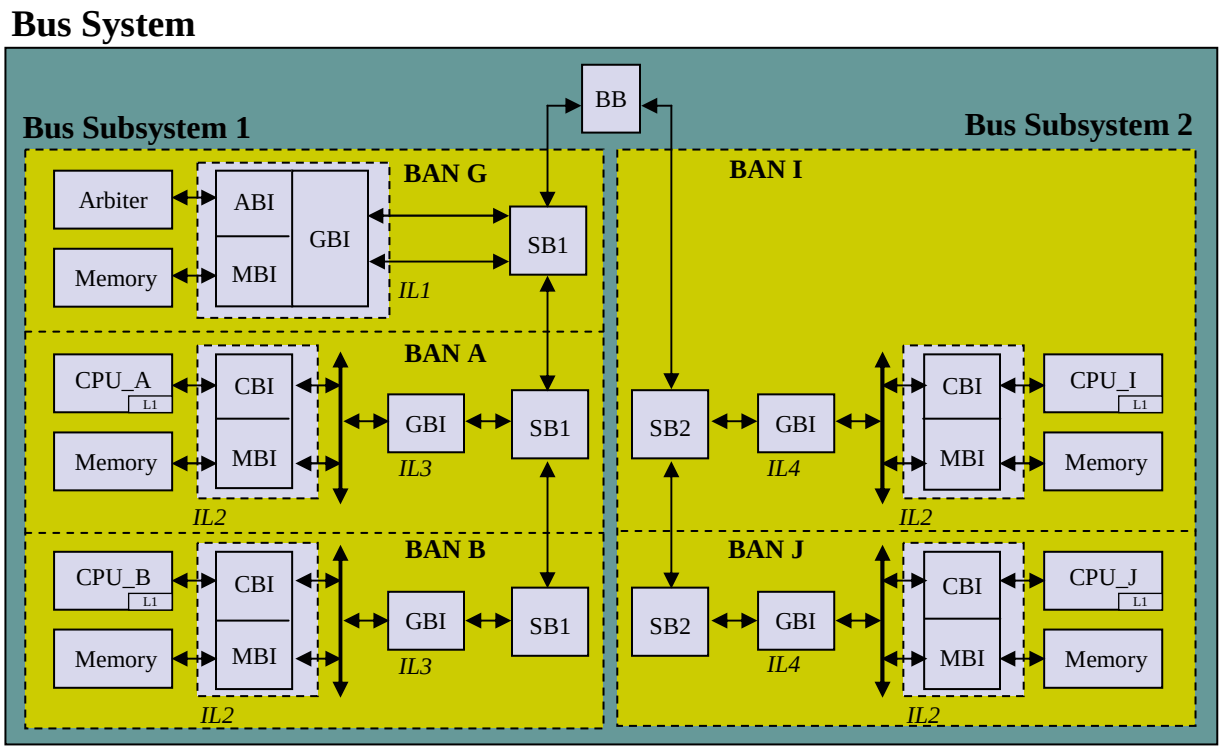
- System-on-a-Chip (SoC)
- Bus Synthesis Goal
  - Easy and Quick Design
  - Design Space Exploration
- Motivation
  - Automated Custom Bus Design
  - Automated Design Space Exploration across Performance Impacting Factors (e.g., type of bus architecture, PEs and programming style



Related Work

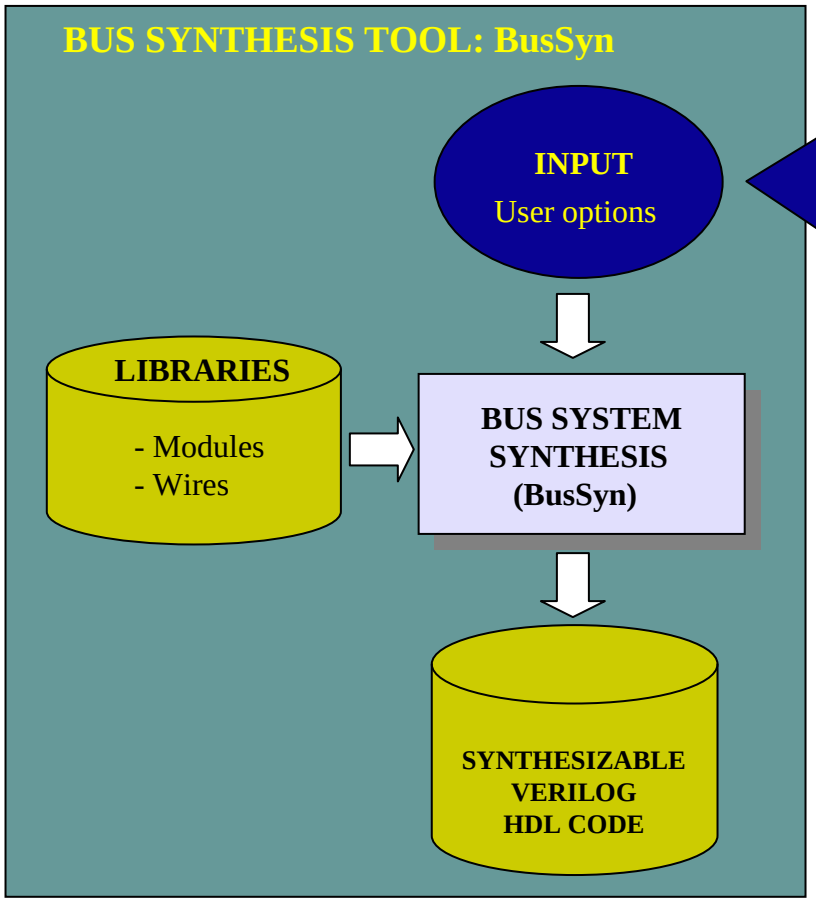
- M. Gasteier *et al*., “Bus-Based Communication Synthesis on System-Level”
  - Automatic generation of communication topologies on system-level
- R.A. Bergamaschi *et al*., “Designing Systems-on-Chip using cores”
  - Assembling an SoC using IP blocks and their properties
- Pai Chou *et al*., “IPCHINOOK: An Integrated IP-based Design Framework for Distributed Embedded Systems”
  - a component-based approach to SoC system building
- TIMA Lab: Component-based Design, Wrapper Generation
- Our Work: Supporting Multiple and Heterogeneous Bus Architectures and Various Wrappers in a System
- SoC Bus Efforts in Industry
  - AMBA from ARM Ltd., CoreConnect from IBM Corp., SiliconBackplane from Sonics Inc. Wishbone from Silicore Corp., CoreFrame from Palmchip Corp.

Bus System Structure



BAN: Bus Access Node, IL: Interface Logic, SB: Segment of Bus, BB: Bus Bridge, MBI: Memory-Bus Interface, CBI: CPU/PE-Bus Interface, GBI: Generic Bus Interface, ABI: Arbiter-Bus Interface,

BusSyn and User Options



User Input List

1. Bus System:
- Number of Bus Subsystems

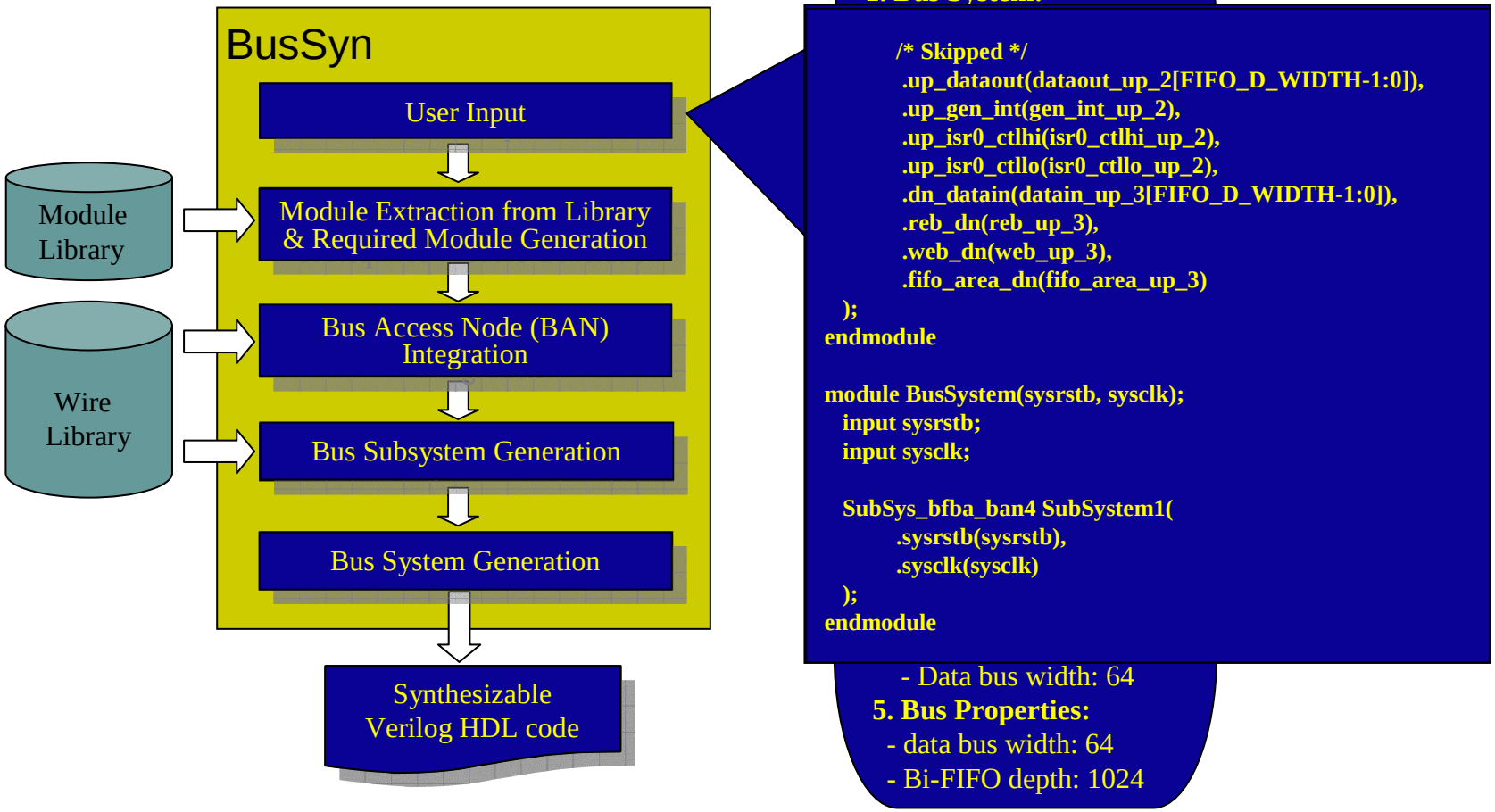
2. Bus Subsystem:
- **For Each Bus Subsystem**
  - Number of BANs:
  - Bus Type: GBAVI, GBAVIII, BFBA, Hybrid or SplitBA

3. BAN Properties:
- **For Each BAN:**
  - CPU Type: MPC750, MPC755, MPC7410 or ARM9TDMI
  - Non-CPU Type: DCT or MPEG2 decoder
  - Number of Memories

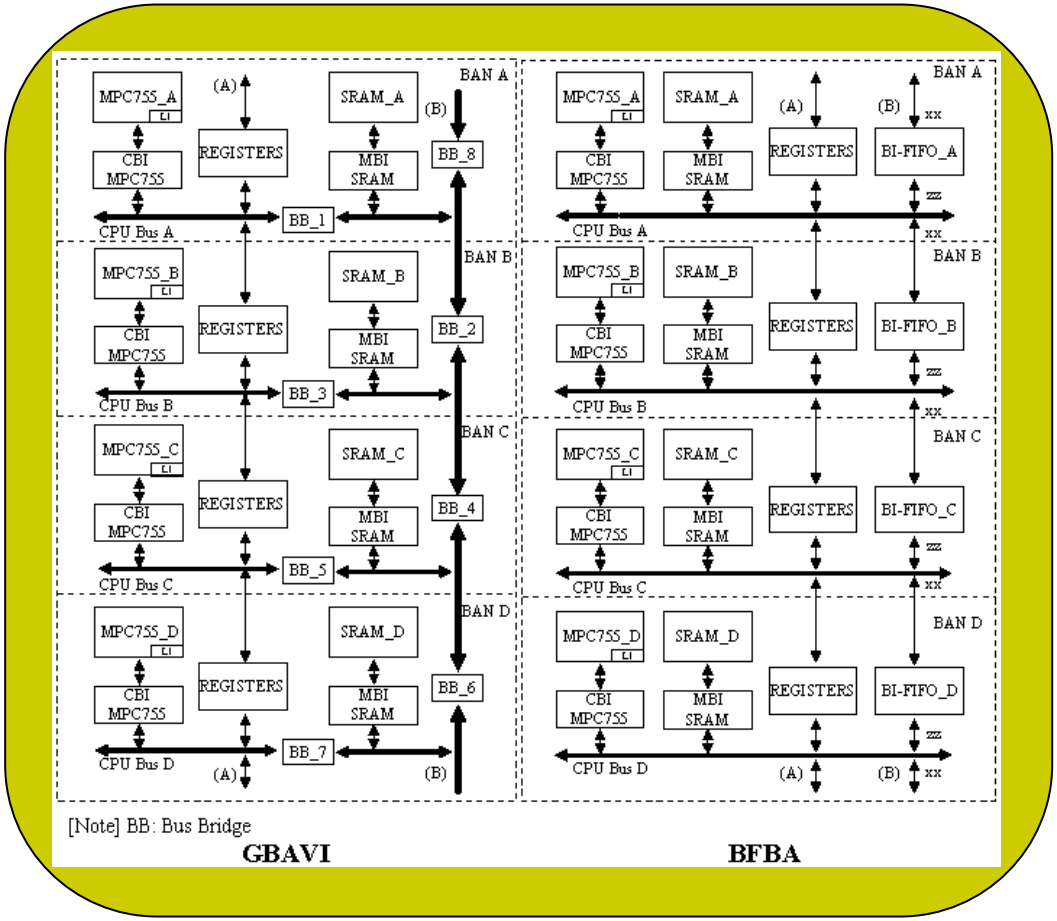
4. Memory Properties:
- **For Each BAN:**
  - **For Each Memory:**
    - Type: SRAM, DRAM, DPRAM or FIFO
    - Address bus width
    - Data bus width

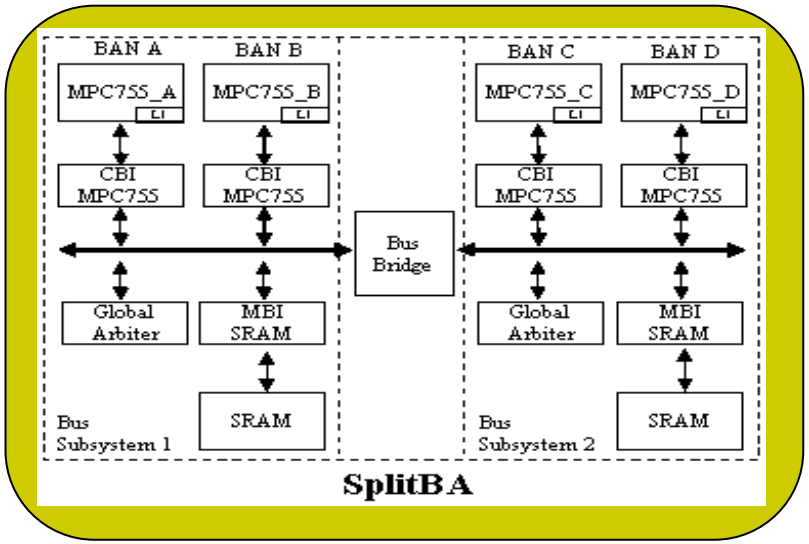
5. Bus Properties:
- **For Each Bus Type**
  - address bus width
  - data bus width
  - Bi-FIFO depth for BFBA and Hybrid

A Bus Generation Sequence with an Example, BFBA

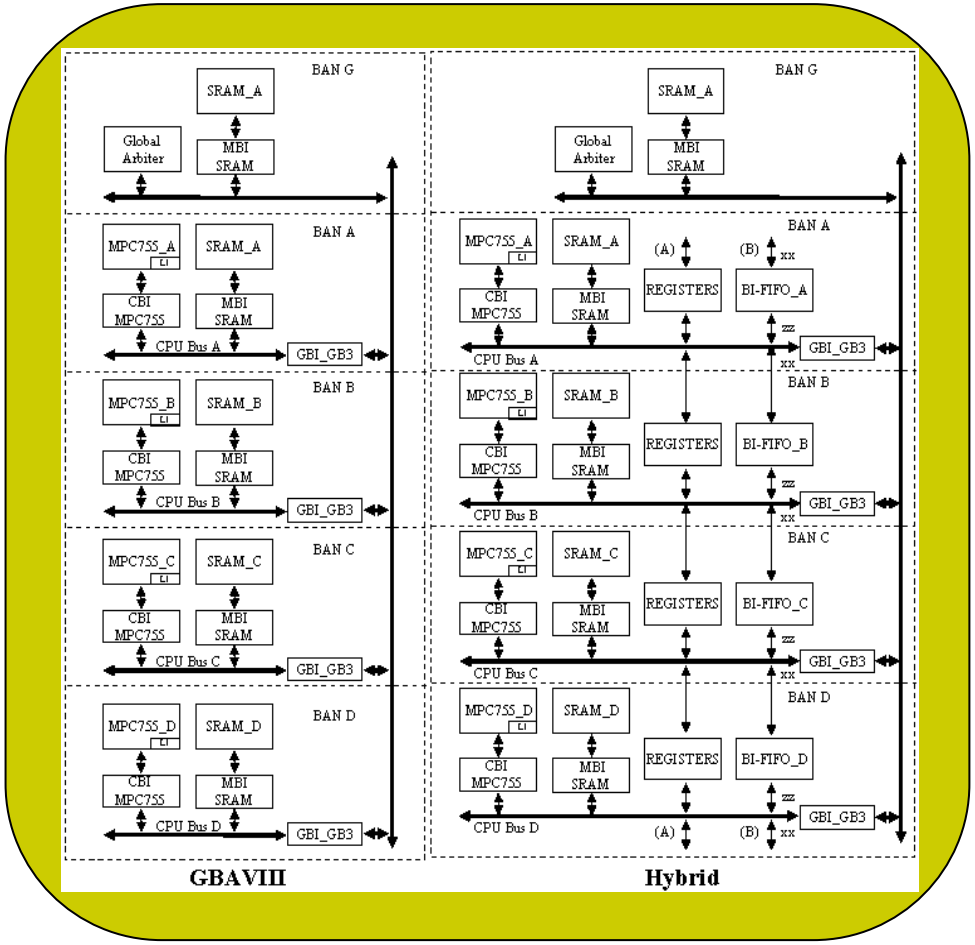


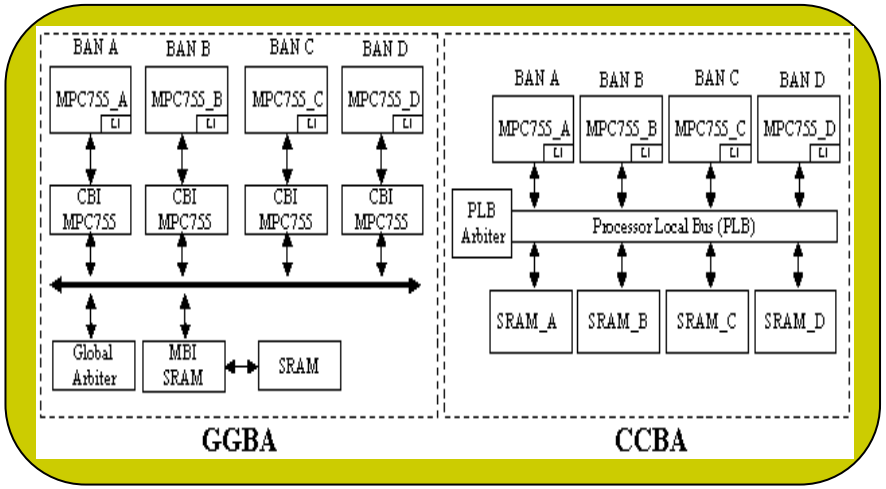
Bus System Examples I





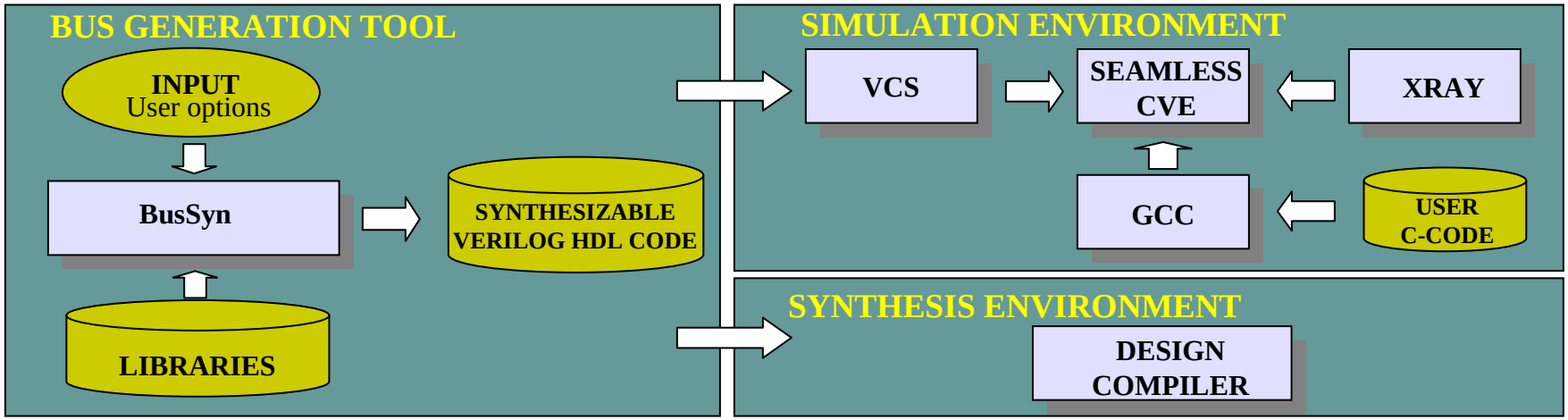
Bus System Examples II





Application Examples and Experimental Environment

- OFDM Transmitter, a Wireless Application
- MPEG2 Decoder
- Database Example, a Multi-thread Example



Note: VCS and Design Compiler from Synopsys, Seamless CVE and Xray from Mentor Graphics and GCC from GNU

Performance Evaluation I

- OFDM Transmitter

Case	Bus System	Throughput [Mbps]	Software Programming Style
1	BFBA	2.6504	PPA
2	GBAVI	2.1087	PPA
3	GBAVIII	4.5599	FPA
4		2.2567	PPA
5	Hybrid	4.5599	FPA
6		2.6504	PPA
7	SplitBA	5.1132	FPA
8	GGBA	4.3913	FPA
9		2.1880	PPA

Note: 1. PPA: Pipelined Parallel Algorithm, FPA: Functional Parallel Algorithm
2. Data: 2048 complex samples and 32 guard complex samples per packet
3. All Bus Systems run on four PowerPCs support instruction and data cache operations

- SplitBA outperforms GGBA by 16.44%
- Bus Systems using a shared memory (e.g.,GGBA) requires more memory arbitration time than in Bus System having separate memory (e.g., GBAVIII)

Performance Evaluation II

- MPEG2 Decoder

Case	Bus System	Throughput [Mbps]
10	BFBA	0.8594
11	GBAVI	0.8271
12	GBAVIII	1.1444
13	Hybrid	1.1650
14	CCBA	1.0083

[Note] 1.Picture size: 16 x 16
2.All Bus Systems run on four PowerPCs have Functional Parallel Algorithm

  - Hybrid shows the best in performance (15.54% against CCBA)

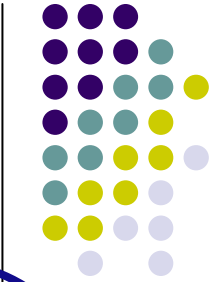
- Database

Case	Bus System	Execution Time [ns]
15	GGBA	2,241,100
16	SplitBA	1,317,804

[Note] 1. Each Bus System is composed of 1 server and 4 clients.
2. The server has 1 task, and the each client has 10 tasks.
3. Each task accesses 100 data to or from the shared memory.

  - SplitBA outperforms GGBA by 41% reduction in time

Summary and Conclusion



- Bus System Structure for Bus System Generation
- Bus System Generation Tool: BusSyn
- BusSyn: How to Generate BANs, Bus Subsystems and Bus System
- Performance Evaluation:
  - SplitBA Shows 16.44% Improvement and 41% Reduction in Time When Compared to GGBA
  - Hybrid Outperforms CCBA by 15.54% in MPEG2 Decoder
- Methodology Benefit