August 18, 2006

Unscrambling the power losses in switching boost converters

**Learn how to effectively balance your use of buck and boost converters and improve the efficiency of your power system
**

By Gabriel A. Rincón-Mora, Senior Member, IEEE, and Neeraj Keskar, Student Member, IEEE, Georgia Tech Analog and Power IC Design Lab

In the expanding world of portable electronic devices, there is no one single parameter more important than battery life, or more important than efficient power conditioning, which is why switching regulators are so popular. Linear regulators may be simpler and less noisy but their switching counterparts are more efficient and therefore preferred, when possible, and while step-down buck switching converters are more efficient, step-up boost converters are often necessary and unavoidable, especially in battery-powered systems. Many designers are therefore confronted with the challenge of decreasing the power losses of a boost switching regulator, and understanding the basic mechanisms that incur power losses and their associated design tradeoffs is key in this regard. Literature on the subject, unfortunately, tends to concentrate on buck converters [1], and the results are often involved and with limited circuit insight. The objective of this article is to perhaps unscramble and hopefully bring insight into the power-consuming mechanisms of a boost converter, establishing the means by which a designer can more effectively balance design choices.

A Typical Boost Converter

A DC-DC boosting function is basically realized by first energizing an inductor in one cycle and releasing the stored energy to the output in the other, as realized by the circuit shown in Figure 1a when switch MN is engaged (MP and D are off) and inductor L is energized (connected from input supply V_{IN} to ground) and later when switches MP and D are on (MN is off) and the energy stored in L is released to the load and output capacitor in the form of a current. Since the average voltage across the inductor in steady state is zero, the average voltage at the switching phase node V_{PH} is equal to V_{IN} and its peak voltage (V_{PK}) is therefore higher than V_{IN}, the latter of which is impressed across output capacitor C via peak detector switch combination MP-D (VOUT ≈ V_{PK}). The *on* time of the circuit is defined as the time interval for which MN conducts and inductor current rises, as shown in Figure 1b, and *off* time alludes to the time when MP-D conduct a decreasing inductor current. Broadly, three basic mechanisms incur power losses in the boost switching converter: conduction losses resulting from switch-on and series parasitic resistances (I^2R), switching losses resulting from current-voltage overlapping events across the switching transistors (when switching node V_{PH} is neither at ground nor V_{OUT}), and gate-drive losses, which amount to the energy required to charge and discharge the gate capacitances of the switching transistors.

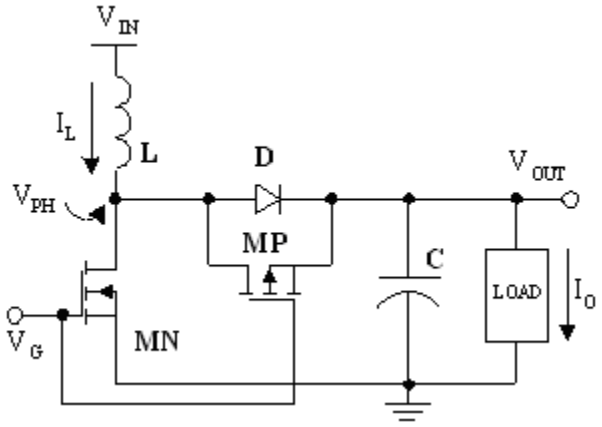

Figure 1a Simplified circuit schematic

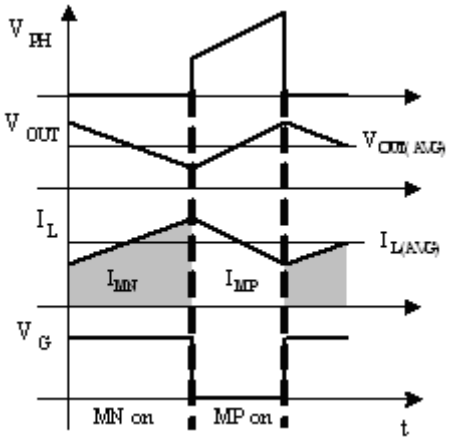

Figure 1b Switching waveforms of a switching boost converter

Conduction losses

To better understand conduction losses, it is helpful to decompose the inductor current into its AC ripple ($I_{L\text{-}RIP}$) and its DC ($I_{L\text{-}AVE}$) components. Generally, however, since inductor current flows to ground during the on time, only a fraction (off time to period ratio) flows to the output, as illustrated by the pulsing currents in Figure 2 (this is the reason why boost converters are generally less power efficient than buck converters). Consequently, the current flowing through switch MN is the inductor current times the on time to period ratio, in other words, duty cycle D times inductor current I_L and the current flowing through MP is its complement, 1-D times I_L. The average component of the MP current flows to the load as I_O,

$$I_{L\text{-}AVE} = \frac{I_{MP\text{-}AVE}}{(1-D)} = \frac{I_O}{(1-D)} \quad \textbf{(1)}$$

and the ripple to capacitor C. The ac ripple current is equivalent to a constant current whose value is the root-mean square (RMS) of the ripple current ($I_{L\text{-}RIP\text{-}RMS}$), which can be shown through simple calculations to be the ratio of the peak-to-peak ripple (ΔI) to the square root of 12 (ΔI/√12) [2]. Given these currents and the nature of their distribution, conduction power losses are simply the product of the squared currents, the percentage of time they flow through a given device, and any and all resistances in their path:

$$P_{IL\text{-}AVE} = I_{L\text{-}AVE}^2 ESR_L + D\left(I_{L\text{-}AVE}^2 r_{MN}\right) + (1-D)\left(I_{L\text{-}AVE}^2 r_{MP}\right) \quad \textbf{(2)}$$

and

$$P_{IL\text{-}AVE} = I_{L\text{-}RIP\text{-}RMS}^2 ESR_L + D\left(I_{L\text{-}AVE}^2 r_{MN}\right) + (1-D)\left(I_{L\text{-}AVE}^2 r_{MP}\right) + (1-D)\left(I_{L\text{-}RIP\text{-}RMS}^2 ESR_C\right) \quad \textbf{(3)}$$

As can be noted, all resistances in the conduction path are critical, especially the switch turn-on resistances and the inductor's equivalent series resistance (ESR), followed by the output capacitor's ESR, the latter of which only carries $I_{L\text{-}RIP\text{-}RMS}$, not $I_{L\text{-}AVE}$.

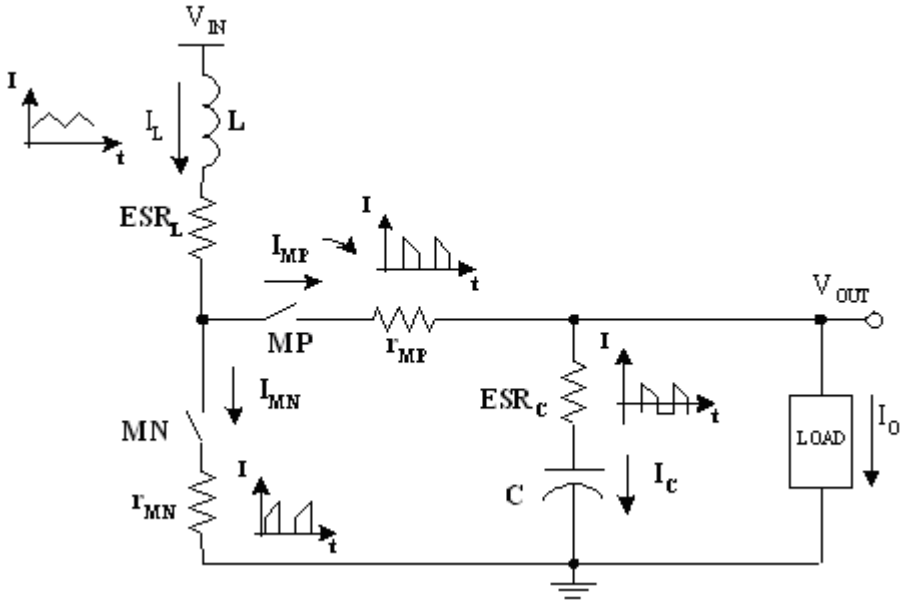

Figure 2. Current composition and distribution across a boost converter

Switching losses

As stated earlier, switching losses refer to the time during which switching node V_{PH} is between its extreme values, when the voltage across the switches is not negligible and current is relatively high. This occurs because, as the switches are engaged or disengaged and current flows through them, the voltage across the terminals of a switch transitions to non-negligible values. The ability of the switch to conduct the full inductor current and decrease the voltage across its terminals is determined by its driving circuit and the parasitic devices surrounding it, as shown in Figure 3a, where an ideal buffer with output resistance and series gate resistance combination R_G drives the parasitic gate-source and gate-drain capacitors of MN (C_{gs} and C_{gd}), and stray capacitance C_d loads MN. Switching losses therefore refer to the power dissipated by MN during turn-on and -off events, when neither MN drain current I_{MN} or MN's V_{ds} voltage V_{PH} is zero.

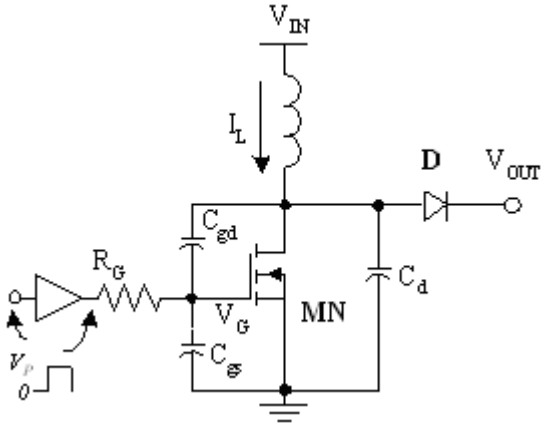

Figure 3a. Equivalent circuit

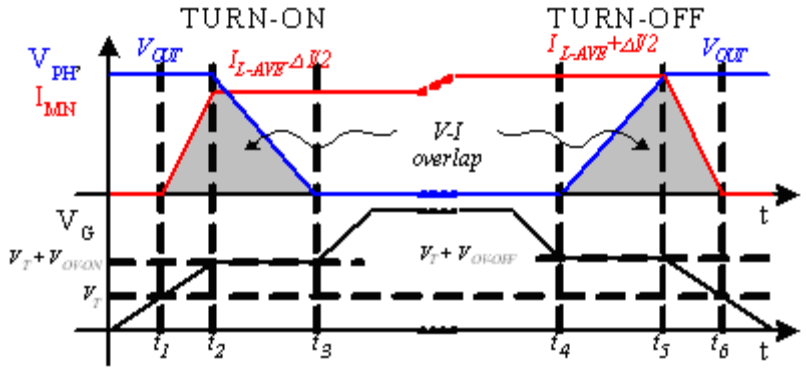

Figure 3b. Relevant switching waveforms of switch MN

Figure 3b illustrates how and when sufficient I_{MN} overlaps V_{PH} (MN's V_{ds}) to cause considerable power losses. For a turn-on event, assuming C_{gd} slews before C_d (that is, C_d is non-dominant), which is typical, MN starts conducting current when the driver charges MN's gate beyond its threshold voltage, as shown in Figure 3b, conducting the full inductor current I_L only when enough overdrive is achieved (that is, $V_{gs} = V_T + V_{OV\_ON}$). Once MN carries all of I_L, MN starts to pull V_{PH} down, essentially starving diode D of current, placing MN in its high gain (saturation) mode, and causing C_{gd} to display the well-known Miller effects. The Miller region manifests itself when small changes in gate-source voltage cause large variations in drain-source voltage (t_{23} in Figure 3b). This region stops when V_{PH} is close enough to ground to pull MN out of saturation and into triode, which for all practical purposes translates to a zero-volt event with no power losses. Similarly, during a turn-off event, the sequence of events is reversed, where excessive overdrive is first attenuated, V_{PH} is raised during a Miller plateau, and the gate is finally pulled below threshold levels. The V-I overlap events that result during these two transitions (shaded region of Figure 3b) result in MN switching losses.

In quantifying the switching power losses, which occur between time intervals t_{13} and t_{46}, it is noted that a switching transition is much faster than the period of the converter, that is, the inductor current is for all practical purposes fixed at one of its peaks during the transition, at $I_{L\text{-}AVE}$-0.5ΔI or $I_{L\text{-}AVE}$+0.5ΔI. Consequently, assuming linear current and voltage transitions (1st order approximation), the switching losses ($P_{SW\text{-}OL}$) amount to the average V-I power dissipated by MN during the on and off transitions:

$$P_{SW\text{-}OL} = 0.5\left(I_{L\text{-}AVE} - 0.5\Delta I\right)V_{OUT}\frac{t_{on\_ir}}{\tau_{sw}} + 0.5V_{OUT}\left(I_{L\text{-}AVE} - 0.5\Delta I\right)\frac{t_{on\_vf}}{\tau_{sw}}$$

$$+0.5\left(I_{L\text{-}AVE} + 0.5\Delta I\right)V_{OUT}\frac{t_{off\_vr}}{\tau_{sw}} + 0.5V_{OUT}\left(I_{L\text{-}AVE} + 0.5\Delta I\right)\frac{t_{off\_if}}{\tau_{sw}}$$

$$= 0.5V_{OUT}\left(I_{L\text{-}AVE} - 0.5\Delta I\right)\left(t_{on\_ir} + t_{on\_vf}\right)f_{sw} + 0.5V_{OUT}\left(I_{L\text{-}AVE} + 0.5\Delta I\right)\left(t_{off\_vr} + t_{off\_if}\right)f_{sw} \quad \textbf{(4)}$$

where times t_{on_ir} (t_{12}) and t_{on_vf} (t_{23}) correspond to the rising I_{MN} and falling V_{PH} of the on transition,
t_{off_vr} (t_{45}) and t_{off_if} (t_{56}) the rising V_{PH} and falling I_{MN} of the off transition, and
τ_{sw} the switching period ($1/f_{sw}$),
all of which is nothing more than the area of the shaded region in Figure 3b. MN switching losses are therefore linearly proportional to peak switching voltage V_{OUT}, inductor peak currents $I_{L\text{-}AVE}$-0.5ΔI and $I_{L\text{-}AVE}$+0.5ΔI, switching frequency f_{sw}, and the transition times of I_{MN} and V_{PH}.

I_{MN} transition times t_{on_ir} and t_{off_if}, as alluded to earlier, depend on how fast the driver is able to charge and discharge the gate when there are no Miller effects. The average on- and off-time gate currents when I_{MN} and V_{PH} transition ($I_{G\text{-}ir\text{-}AVE}$, $I_{G\text{-}if\text{-}AVE}$, $I_{G\text{-}vf\text{-}AVE}$, and $I_{G\text{-}vr\text{-}AVE}$ for I_{MN} rising and falling and V_{PH} falling and rising, respectively), to a first order approximation, can be estimated to be the average voltage across R_G divided by R_G,

$$I_{G-tr-AVE} \approx \frac{V_P - (V_T + 0.5V_{OV-ON})}{R_G} \quad \textbf{(5)}$$

$$I_{G-tf-AVE} \approx \frac{V_T + 0.5V_{OV-OFF}}{R_G} \quad \textbf{(6)}$$

$$I_{G-vf-AVE} \approx \frac{V_P - (V_T + V_{OV-ON})}{R_G} \quad \textbf{(7)}$$

and

$$I_{G-vr-AVE} \approx \frac{V_T + V_{OV-OFF}}{R_G} \quad \textbf{(8)}$$

where V_{OV-ON} and V_{OV-OFF} are the overdrive voltages required to sustain peak currents I_{L-AVE}-ΔI/2 and IL-AVE+ΔI/2. Because these currents slew C_{gs} and C_{gd} during I_{MN} transitions and C_{gd} during V_{PH} transitions (Miller plateau), their respective times are

$$t_{sw\_on} = t_{tr-tr} + t_{tr-vf} \approx \frac{(C_{gs}+C_{gd})\Delta V_{gs}}{I_{G-tr-AVE}} + \frac{C_{gd}\Delta V_{ds}}{I_{G-tf-AVE}} = \frac{(C_{gs}+C_{gd})V_{OV-ON}R_G}{V_P-(V_T+0.5V_{OV-ON})} + \frac{C_{gd}V_{OFF}R_G}{V_P-(V_T+V_{OV-ON})} \quad (\mathbf{t_{sw\_on}})$$

$$t_{sw\_off} = t_{tf-tf} + t_{tf-vr} \approx \frac{C_{gd}\Delta V_{ds}}{I_{G-tf-AVE}} + \frac{(C_{gs}+C_{gd})\Delta V_{gs}}{I_{G-tr-AVE}} = \frac{C_{gd}V_{OFF}R_G}{V_T+V_{OV-OFF}} + \frac{(C_{gs}+C_{gd})V_{OV-OFF}R_G}{V_T+0.5V_{OV-OFF}} \quad (\mathbf{t_{sw\_off}})$$

The end result is that MN switching losses also increase with larger parasitic capacitors C_{gs} and C_{gd} and overdrive voltages V_{OV-ON} and V_{OV-OFF}, and lower gate-drive currents.

While the drain-source voltage extremes of MN's V-I overlap losses are between zero and V_{OUT}, the extremes for MP are zero and a diode voltage (V_D), which incur significantly reduced and often negligible V-I power losses when compared to MN (same phenomenon but with V_D in place of V_{OUT} in Equation 4). The reason for this limited voltage swing is deadtime, which is intentionally introduced to prevent MN and MP from simultaneously conducting current (prevent shoot-through current) and wasting power. Consequently, when MN turns off, diode D freewheels and clamps the voltage across MP to V_D before MP is allowed to turn on. Conversely, MP is turned off before MN is allowed to conduct current, causing diode D to again carry the inductor current. Although these V-I losses can be neglected, excessive deadtime incurs additional power losses across the diode and may in the end affect the overall efficiency performance of the converter, if not in check,

$$P_D = V_D(I_{L-AVE} - 0.5\Delta I)\left(\frac{t_{Deadtime\_on}}{\tau_{sw}}\right) + V_D(I_{L-AVE} + 0.5\Delta I)\left(\frac{t_{Deadtime\_off}}{\tau_{sw}}\right) \approx V_D I_{L-AVE}\left(\frac{t_{Deadtime}}{\tau_{sw}}\right) \quad \textbf{(9)}$$

In cases where C_d is greater than about five times C_{gd}, like in snubbers, both C_{gd} and C_d slew, not just C_{gd}, as is normally the case (assumption in analysis above). The voltage across C_{gd} and the ensuing changes in gate-source voltage V_{gs} determine the magnitude of C_d's slewing current. In essence, the V_{PH} rising and falling rates transition from C_{gd}- to C_d-slew dominant, ultimately slowing down the response to where the driving gate current (that is, R_G) is no longer a factor. Figure 4, for instance, illustrates how the falling rate of V_{PH} ($\partial V/\partial t$) of a nominal n-type MOS switch with a transconductance of 2 s and gate-drain capacitance of 4 pF remains fairly constant for low-to-moderate values of C_d, increases for values greater than five times C_{gd}, and becomes independent of R_G for large values of C_d.

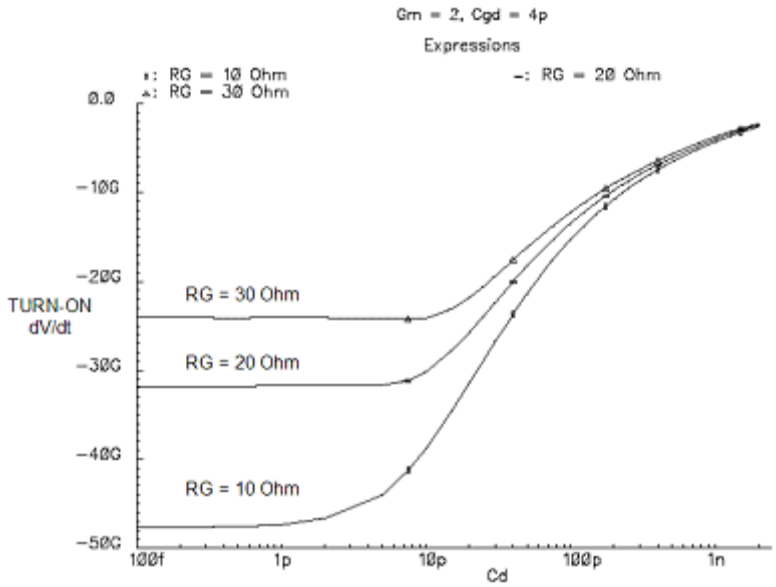

Figure 4. Effects of drain capacitance C_d on the falling rate of switching node V_{PH}

Gate-drive losses

Gate-drive losses refer to the energy required to charge and discharge the gate-source and gate-drain capacitances of the switches, which is directly proportional to switching frequency f_{sw}, capacitance, and the square of the voltage traversed. MN's C_{gs}, for instance, in battery-powered applications, is typically driven by a driver powered from input supply V_{IN}, causing the gate to charge and discharge the full supply, between V_{IN} and ground. MP's C_{sg}, on the other hand, is driven between V_{OUT} and ground because the only way to turn off the PMOS is to drive its gate voltage close to its source, which in this case is the output. MN's C_{dg}, however, charges from "V_{IN} (MN is on) to V_{OUT} (MN is off), incurring a total voltage swing of V_{IN} + V_{OUT}, whereas MP's C_{dg} swings from -V_{OUT} (MP is on) to V_{OUT} ($2V_{OUT}$ swing). In the end, the total power lost in charging and discharging gate capacitances is given by

$$P_{GT} = \frac{1}{2}\left[C_{gs\_MN}V_{IN}^2 + C_{dg\_MN}(V_{IN}+V_{OUT})^2 + C_{sg\_MP}V_{OUT}^2 + C_{dg\_MP}(2V_{OUT})^2\right]f_{sw} \quad \textbf{(10)}$$

Summary

To start, since the inductor current is not always flowing to the load, the efficiency of boost converters is generally lower than their bucking counterparts. In absolute terms, however, conduction losses refer to the square RMS current flowing through a resistor, the percentage of time that it flows, and the resistance, and when viewed within the context of DC-DC converters, amount to how the average and RMS ac ripple inductor currents are distributed within the circuit, through ESRL and MN during the on time and ESRL and MP-D during the off time, plus the ac current portion that flows into ESR_C. Switching V-I overlap losses for the pull-down NMOS are larger than for the PMOS because of deadtime and diode D, which limit the voltage swing across the PMOS switch to V_D, as opposed to V_{OUT}, as in the case of the NMOS, which is why the total V-I losses are approximately set by MN, by V_{OUT}, inductor current I_L, voltage-current transition times (that is, gate drive), and switching frequency f_{sw}. Drain capacitance on switching node V_{PH} slows down the transition and consequently increases power losses, but the power loss is normally negligibly small, when compared to other factors, except when intentional drain capacitance is introduced (when C_d is greater than $5C_{dg}$). There is also some power dissipated during deadtime, when inductor current flows through the diode, which is proportional to the diode voltage, inductor current, and the percentage of time it flows during each cycle. Gate-drive losses refer to the energy required to charge and discharge all gate-source and gate-drain capacitances, and they are proportional to capacitance, switching frequency, and the square of the voltage transition. Although exact relationships for all the power losses are often desired, the foregoing analysis may prove more useful in a design environment, where critical design choices are made a priori and later verified and tweaked with simulators like Cadence.

For additional details, questions, and/or comments on this article, please contact us, the Georgia Tech Analog and Power IC Design Laboratory, at gtap@ece.gatech.edu. More information about our research can be found at http://www.rincon-mora.com/research.

References

[1] M. Gildersleeve, G.A. Rincón-Mora et al, "A comprehensive power analysis and a highly efficient, mode-hopping DC-

DC converter," IEEE Asia-Pacific Conference on ASIC, 2002, pp. 153-156.
[2] G.A. Rincón-Mora, Power Management ICs - A Top-Down Design Approach, ISBN: 1-4116-6359-4.