Static Random Access Memory

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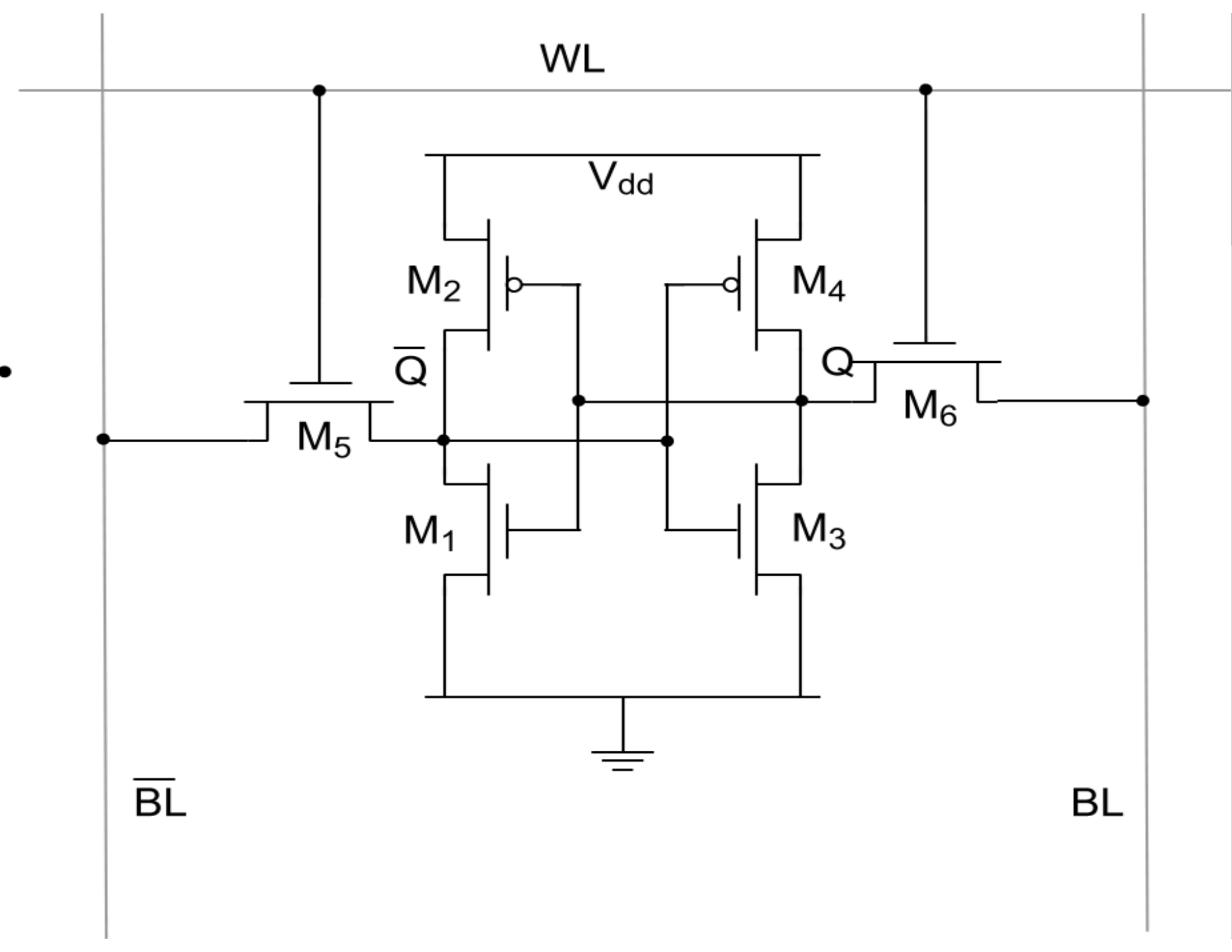
Overview

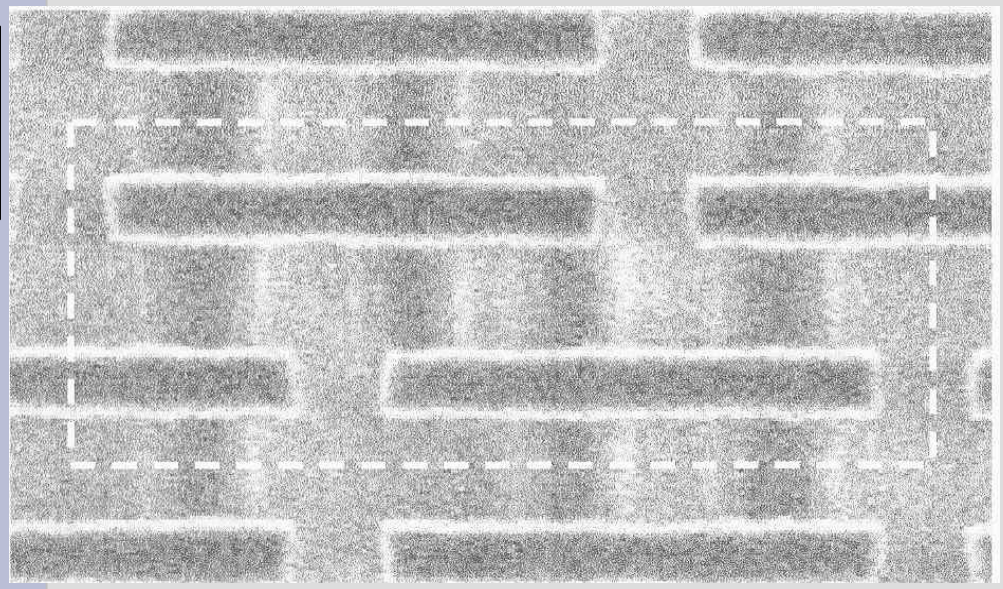
- What is SRAM?
- What is SRAM used for?
- Where is SRAM going in the future?

What is SRAM?

- SRAM occupies a middle ground between DRAM and the various types of ROM
- Does not need to be refreshed constantly like DRAM, is also faster than DRAM
- Will not hold data without power, unlike ROM
  - At least not for more than 100s of ms
  - Data loss rate is inversely related to temperature and current
- The most common form today uses 6 MOSFETs

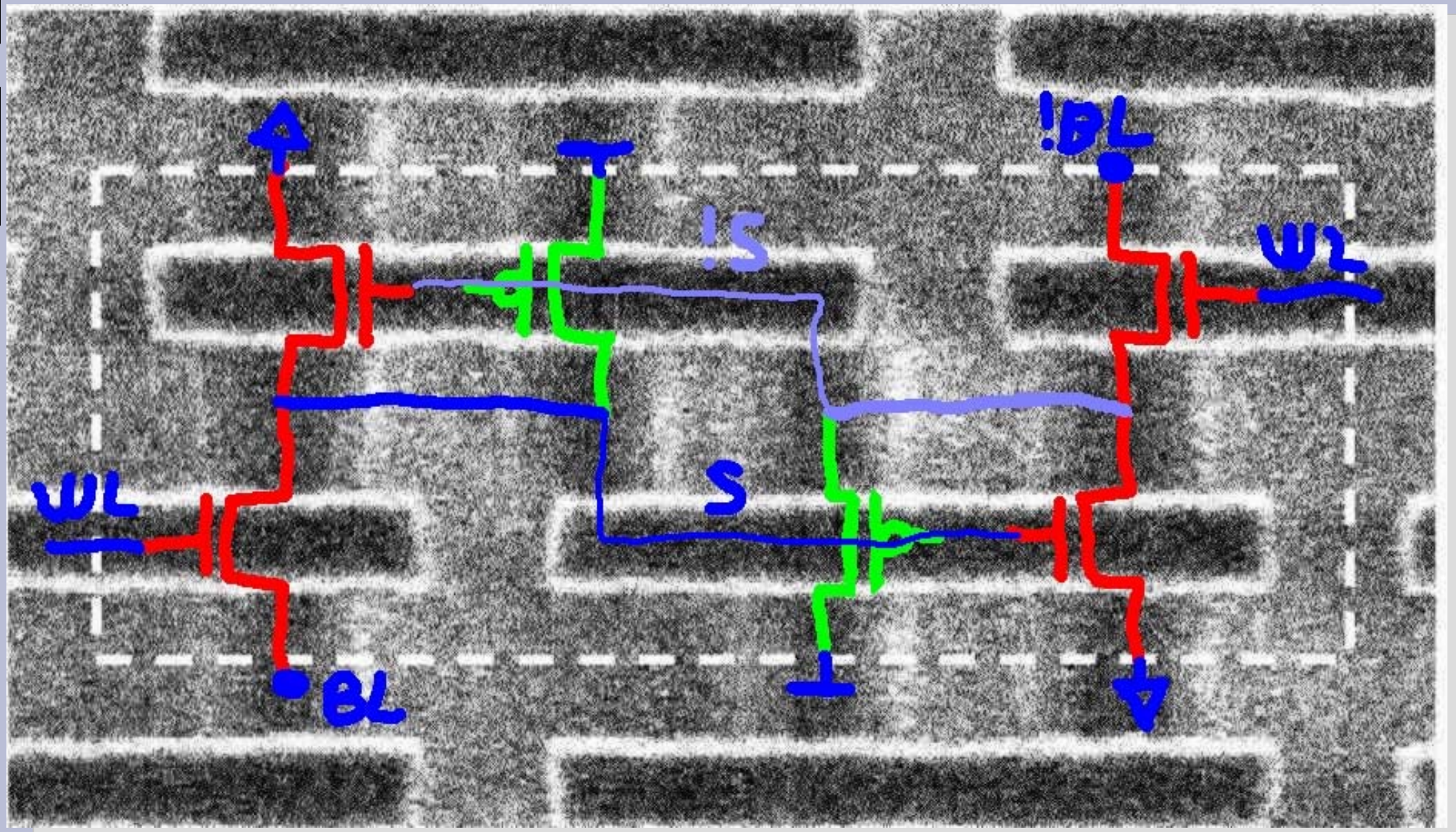

WL
V_{dd}
M_2
M_4
$\overline{Q}$
Q
M_5
M_6
M_1
M_3
$\overline{BL}$
BL

SRAM in Silicon



- This cell (outlined area) was made on intel's 45nm process
- It has an area of 0.346 um^2
- The latest 32nm processes give SRAM cells with an area of 0.15 um^2

Labeled 45nm SRAM Cell



Static Noise Margin

- Measures the voltage needed to make the cell change state
- Inversely related to cell size

- For a 6T SRAM cell, the SNM is given by:

$$\mathrm{SNM}_{6T} = V_T - \left(\frac{1}{k+1}\right)\left\{\frac{V_{DD} - \frac{2r+1}{r+1}V_T}{1+\frac{r}{k(r+1)}} - \frac{V_{DD}-2V_T}{1+k\frac{r}{q}+\sqrt{\frac{r}{q}\left(1+2k+\frac{r}{q}k^2\right)}}\right\}$$

Sorry, I lied...

- That equation is not very useful for modern and future SRAM
  - The paper it's from is from 1987, when 3V CMOS was cutting edge
- SRAM now operates at voltages below the threshold voltage
  - Usually around or below 1V
- The main factor affecting SNM is now random doping variation

What is SRAM used for?

- Embedded cache for microprocessors
  - In modern desktop processors, SRAM can be as much as 50% of the die by area
- Memory
  - When the amount needed is too small to justify the increased complexity of DRAM
  - Most modern consumer electronics
- Process validation
  - Simple, repeatable design, easy to test for defects

The Future of SRAM

- Smaller and smaller processes
  - Intel is already developing a 22nm process – expected to be ready by 2011
  - Smaller processes will allow 8T SRAM designs to be used to reduce leakage currents
- 3D/stacking
- Designs based on more advanced transistors
  - FinFET-based designs show a 30-70% improvement in SNM over 6T SRAM
  - FinFETs also scale better to smaller processes

Questions?

Sources

- http://en.wikipedia.org/wiki/Image:6t-SRAM-cell.png
- http://www.realworldtech.com/includes/images/articles/iedm-2007-2.gif
- http://ctho.ath.cx/pics/45nm_SRAM_Cell_labeled.jpg
- http://mtlweb.mit.edu/researchgroups/icsystems/pubs/conferences/2005/bcalhoun_esscirc2005_paper.pdf
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