COURSE DETAILS AND INFORMATION FOR ECE6440 – FREQUENCY SYNTHESIZERS

Instructors: Dr. Phillip E. Allen, Room 292B, Van Leer, 894-6251 (office), (404) 603-9374 (home), pallen@ece.gatech.edu

Lecture: Monday, Wednesday, and Friday, 10:40am to 11:50am, Room C456, Van Leer

Office Hours: Allen: 2-3pm, MW, 2:30-3pm F or by e-mail <pallen@ece.gatech.edu>.

Electronic Copies of Class Handouts: You may download pdf copies of all classroom material at the following web site: http://users.ece.gatech.edu/~pallen/Academic/

Texts:

Unfortunately, there is no one single good text for this class. The lecture notes will be taken from the following references. You should refer to these reference for more detail than given in the lecture.

1.) U. L. Rohde, *Microwave and Wireless Synthesizers – Theory and Design*, Wiley Interscience, 1997.

2.) R.E. Best, *Phase-Locked Loops – Design, Simulation, and Applications*, 4th-edition, McGraw-Hill, 1999.

3.) J. Craninckx and M. Steyaert, *Wireless CMOS Frequency Synthesizer Design*, Kluwer Academic Publishers, 1998.

4.) H. Rategh and T.H. Lee, *Multi-GHz Frequency Synthesis and Division*, Kluwer Academic Publishers, 2001.

5.) A. Hajimiri and T.H. Lee, *The Design of Low Noise Oscillators*, Kluwer Academic Publishers, 1999.

6.) B. Razavi, *Design of Integrated Circuits for Optical Communications*, McGraw-Hill, 2003.

7.) Paul Gray, Paul Hurst, Steve Lewis and Robert Meyer, *Analysis and Design of Analog Integrated Circuits – Fourth Edition*, John Wiley and Sons, Inc., 2001

8.) P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design – Second Edition*, Oxford University Press, 2002.

9.) B. Razavi, *RF Microelectronics*, Prentice-Hall PTR, NJ, 1998.

10.) T.H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, NY, 1998.

11.) B.D. Muer and M. Steyaert, *CMOS Fractional-N Synthesizers-Design for High Spectral Purity and Monolithic Integration*, Kluwer Academic Publishers, 2003.

Objectives: The purpose of this course is to develop an understanding of the theory and design of frequency synthesizers using both discrete and integrated technology.

Examinations: There will be two, closed book midterm examinations each of 70 minute duration and a 3 hour final examination. The final examination will be given during the regularly scheduled time for the final exam. All exam grades become final one week after they are returned in class. The midterm exams are scheduled for Monday, June 16, 2003 and Friday, July 18, 2003. The final exam is scheduled for Monday, July 28, 2003, from 2:50pm to 5:40pm.

Homework: Homework will be assigned and will be graded.

Course Projects: There will be two course projects assigned during the semester. One will be a discrete frequency synthesizer design and the other will be a report on a published integrated circuit frequency synthesizer.

Course Grading Policy: Your grade will be determined using the following scheme:

Two midterm exams…..……	40%
Homework……	10%
Course projects…….	20%
Final Exam……	30%

Grades will be assigned on a curve and will not necessarily be consistent with 100>A>90, 90>B>80, etc..

Computer Usage: You are expected to be able to use HSPICE or PSPICE for classroom assignments. Most assignments using the computer will work on the student version of PSPICE. The educational version of PSpice for the PC is free and downloadable from: http://www.orcad.com/products/pspice/eval_f.htm

Attendance: You are responsible for all course materials, announcements, notes, etc. made during our regular class meeting times. Prompt arrival to class is appreciated.

Academic Honesty: It is the responsibility of the instructor to encourage an environment where you can learn and your accomplishments will be rewarded fairly. Any behavior that compromises the basic rules of academic honesty as described in the General Catalog will not be tolerated.

Classroom Behavior: Smoking, drinking and eating is prohibited in the classroom by Institute rules.

Weekly Coverage of Topics for ECE6440

Week	Date	Lect. #	Topic	Reference
1	5/12	010	Introduction to Frequency Synthesizers	[All]
	5/14	020	Discrete Technology for Frequency Synthesizers	[7.8]
	5/16	030	Integrated Technology for Frequency Synthesizers	[7,8,9]
2	5/19	040	Integrated Technology for Frequency Synthesizers	[7,8,9]
	5/21	050	Linear Phase Locked Loop	[2]
	522	060	Linear Phase Locked Loop-Continued	[2]
3	5/26	-	Holiday	[2]
	5/28	070	Digital Phase Locked Loops (DPLL)	[2]
	5/30	080	DPLL-Continued	[2]
4	6/2	090	All Digital Phase Locked Loops (ADPLL)	[2]
	6/4	100	Phase Locked Loop Measurements	[2]
	6/6	110	Phase-Frequency Detectors (PFD)	[2,6]
5	6/9	120	Filters and Charge Pumps	[3,6,9]
	6/11	130	Voltage controlled oscillators (VCOs)	[4,6,9]
	6/13	140	Voltage controlled oscillators (VCOs)	
6	6/16	150	VCOs – Continued	[4,6,9]
	6/18	-	Exam No. 1	
	6/20	160	Low phase noise VCOs	[4,6,9]
7	6/23	170	Phase Noise	[4]
	6/25	180	Phase Noise – Continued	[4]
	6/27	190	Jitter Noise	[4]
8	6/30	200	Frequency Dividers	[6,9]
	7/2	210	Frequency Dividers – Continued	[6,9]
	7/4	-	Holiday	
9	7/7	220	Frequency Synthesizers	[1,3,4,9,11]
	7/9	230	Frequency Synthesizers – Continued	[1,3,4,9,11]
	7/11	240	Frequency Synthesizers - Continued	[1,3,4,9,11]
11	7/14	250	All Digital Frequency Synthesizer for Bluetooth	
	7/16	260	Clock and Data Recovery Circuits	[6]
	7/18	-	Exam No. 2	
12	7/21	270	Clock and Data Recovery Circuits	[6]
	7/23	280	Clock and Data Recovery Circuits	[6]
	7/25	-	Review	
The final exam is scheduled for Monday July 28, 2003, from 2:50pm to 5:40pm.				