Design Problem 1

Due Date: In class, Friday, July 11, 2003

Description:

You are to design a digital-PLL frequency synthesizer covering the frequency range of 1200-1800 MHz in 40 kHz steps. The synthesizer is to be frequency modulated by injecting a voltage into the VCO input. The modulation bandwidth is the voice frequency range of 300 Hz to 3000 Hz. The modulation is to have a 15 kHz peak deviation. A Motorola MC145152-2 parallel-input synthesizer circuit is to be used. The internal reference oscillator of the MC145152-2 integrated circuit together with a Wireless Radio VCO V2-1140 are to be used in the design. The detailed design specifications are listed below.

I. Design Specifications:

1.) Frequency range: 1200-1800 MHz

2.) Channel spacing: 40 kHz

3.) FM deviation: 15 kHz

4.) Loop: Initial design using type-2, second-order. Analyze the design as type-2, third order.

5.) Loop bandwidth: Set by the modulation requirement.

6.) Damping factor: $0.75 \leq \zeta \leq 1.0$

7.) Phase margin: $\geq 55°$

8.) Reference modulation sidebands: $\leq$ -70 dBc

9.) Phase noise: VCO noise to be evaluated

10.) Dual-Modulus prescaler MC12054A (128/129)

11.) Reference oscillator: Use the oscillator built into the MC145152-2.

12.) Loop filter: Perfect integrator with additional filtering by an input passive lowpass filter. Use a Burr-Brown OPA227P,U precision op amp. The minimum allowable value for $R_1 = 2.5$ kΩ.

13.) Power supply: +5V for the MC145152-2 and the MC12054A, ±12V for the loop filter and +10V for the VCO.

14.) Phase detector gain: $V_{DD}/(2\pi) = 0.796$.

15.) Loop expansion factor: $\beta = 2\pi$.

16.) VCO gain: 90×10^6 Hz/V

17.) VCO phase noise: See VCO V2-1140 data sheet.

II. Circuit

A simplified block diagram is shown in Figure 1. You should provide a more detailed circuit diagram for your design.

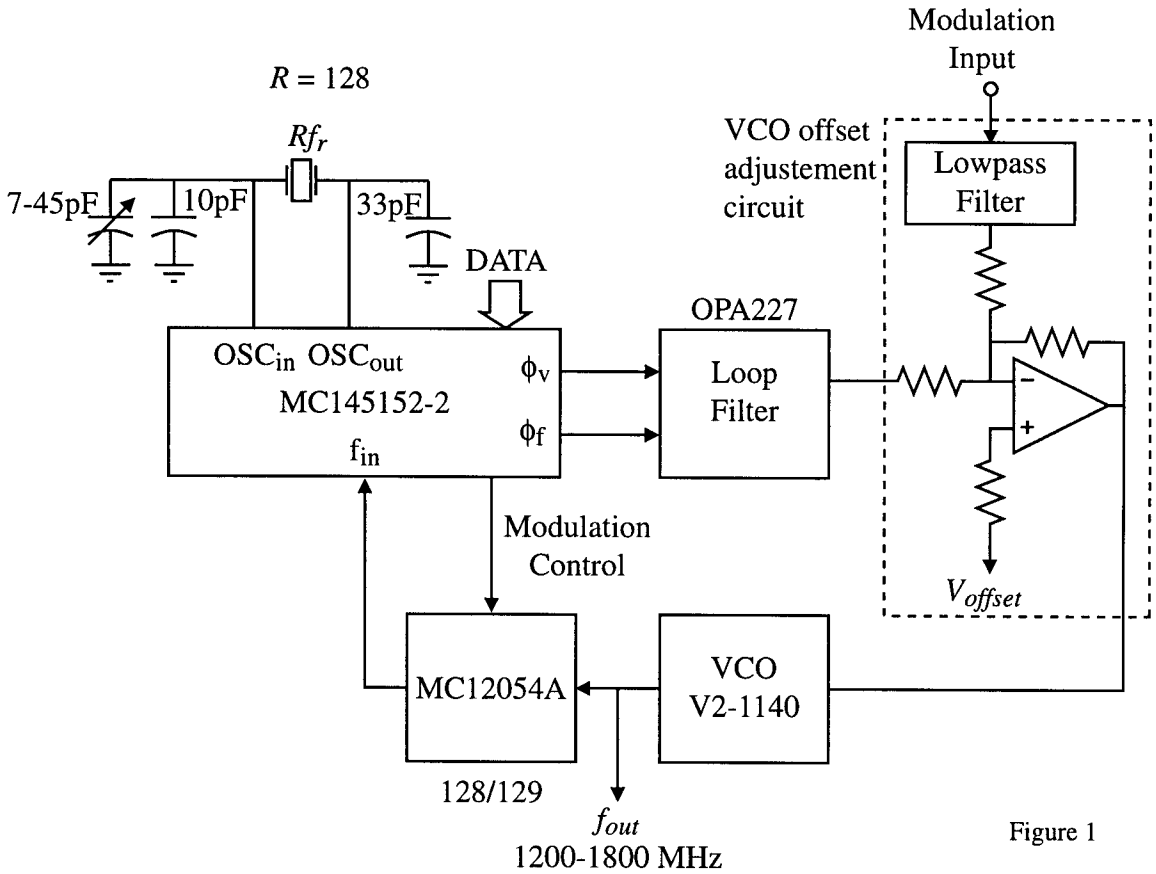


Figure 1

Figure 1 – Block diagram of the 1200-1800 MHz frequency synthesizer.

III. Additional Requirements, Information and Design Hints

1.) Do an initial design for a type-2, second-order system. Derive an equation for the FM modulation bandwidth to determine the proper natural frequency. Once your second-order design is complete, check the reference frequency modulation of the VCO. If it is not satisfactory, add a passive lowpass filter to the input of the loop filter. The addition of the filter changes the system to third order. Next, recheck the reference frequency modulation and check the phase and gain margins of the loop. If these are satisfactory, no compensation or additional filtering is needed.

2.) Specify the voltage for the VCO offset adjust circuit that places the free-running frequency in the center of the VCO frequency range.

3.) You are encouraged to write calculator and/or computer programs that will be useful in the synthesizer design. PSPICE, MATLAB, MathCAD, etc. are general purpose programs that may be useful to you. You must include a copy of your programs or PSPICE data files as an appendix to your report.

4.) You are to do the entire report independently of other students in the class.

V. Report

The results of this design problem are to be presented in a format that is appropriate for an engineering project report. The report of the design should: (1) give the specifications and performance of the design; (2) provide adequate information so that a prototype of the circuit can be built by a technician; (3) explain your design procedure in a manner that can be understood by a technically competent engineer; and (4) provide detailed documentation of your work including any calculator or computer programs. In order to convey this information the report must be organized as as described in the following.

I. Specifications and Performance

1.) The first item in your report should be a statement of the goals of the design and how your design compares with the specifications. Give your calculated reference suppression, gain margin, modulation bandwidth, and compare these with the specifications. Also calculate important quantities such as the lock-in time and lock-in range. This section is a short tabular summary. Finally, present a plot of the VCO phase noise in the output of the synthesizer.

2.) The next item should be a completed circuit diagram of your synthesizer including as much detail as you have available. Please select the nearest 5% tolerance resistors for your circuit. You may assume that capacitors are available with the following progression of values over a decade (1.0, 1.5, 2.2, 3.3, 4.7, 6.8, 10.0, etc.).

3.) Next, provide the following specific items:

a.) A transient analysis of your loop in response to a reference frequency step equal to the capture (lock-in) range. Give the Phase error as a function of time. Compare this value with that predicted from the capture-time equation. Take the simulated capture time as the time for the phase error to decay to 0.1 radian. Do the simulation for both the second- and third-order systems. Adjust scale factors to get reasonable plots.

b.) A plot of the frequency deviation (Δf_{out}) at the output of your loop (as a function of the modulating frequency) in response to the frequency modulation of the VCO. Set your modulating voltage to give the correct deviation for frequencies in the flat region of the transfer function. You should include both second-order and third-order calculations. Use a logarithmic frequency scale.

c.) Present the Bode plots that you used to determine the phase and gain margins. Indicate on the plots the phase and gain margins.

II. Design Methods and Procedures

Next, describe the procedure that you used to arrive at your design. Any particular problems encountered should be discussed here. If your design did not meet specifications, explain what you think is wrong in this section. Items to be included in this section are:

1.) A step-by-step description of the procedure that you followed to create your design.

2.) The procedure that you used to evaluate the performance of your design.

3.) If your design did not meet specifications, an explanation of why and how it could have been modified to meet specifications.

III. Details of the Design

This is the documentation section of the report. In general, this section should provide the mathematical justification for the conclusions summarized in Section I using the methods outlined in Section II. This section would be read by the engineer wishing more detail on some aspect of your design.

IV. Appendix.

The appendix should include copies of all computer and calculator programs used in your work. If you include the problem statement sheet in your report, it should be placed in the appendix, not in the text.

V. References

You should list all references, web sites, and any other sources of information that you used in the preparation of this report.

Grading of the Design Problem

The design problem will be evaluated with respect to three standards. They are (1.) technical accuracy and methods, (2) format, and (3) readability and neatness. The grading criteria are discussed in more detail in the following.

1.) Technical Accuracy and Methods (50%)

The design must meet all design specifications, be accomplished using the specified methods and include all required calculations. If you design does not meet specifications, that fact must be pointed out and an attempt should be made to find any errors.

2.) Format (25%)

Your report must follow the format outlined above. Failure to provide the requested information in the order indicated will cause loss of points in this category.

3.) Readability and Neatness (25%)

Your report must be neat and readable. All schematic diagrams should be made with drawing instruments or some computer-aided drawing package. Make sure your graphs are properly labeled. If is not necessary to type the report, but please make sure that the report is legible and easy to handle. Work done on scratch paper or on sheets torn from spiral-bound notebooks will not be accepted. Errors in English grammar or spelling will be including in the grading. You are encouraged to submit your report electronically if you wish to do so.

MC145152-2

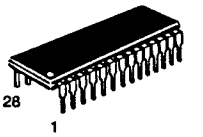
Parallel-Input PLL Frequency Synthesizer

Interfaces with Dual–Modulus Prescalers

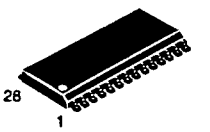
The MC145152–2 is programmed by sixteen parallel inputs for the N and A counters and three input lines for the R counter. The device features consist of a reference oscillator, selectable–reference divider, two–output phase detector, 10–bit programmable divide–by–N counter, and 6–bit programmable ÷ A counter.

The MC145152–2 is an improved–performance drop–in replacement for the MC145152–1. Power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- 8 User–Selectable ÷ R Values: 8, 64, 128, 256, 512, 1024, 1160, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 63
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates
- See Application Note AN980



P SUFFIX
PLASTIC DIP
CASE 710

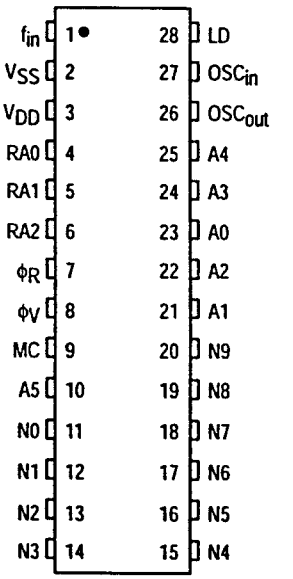


DW SUFFIX
SOG PACKAGE
CASE 751F

ORDERING INFORMATION

MC145152P2	Plastic DIP
MC145152DW2	SOG Package

PIN ASSIGNMENT



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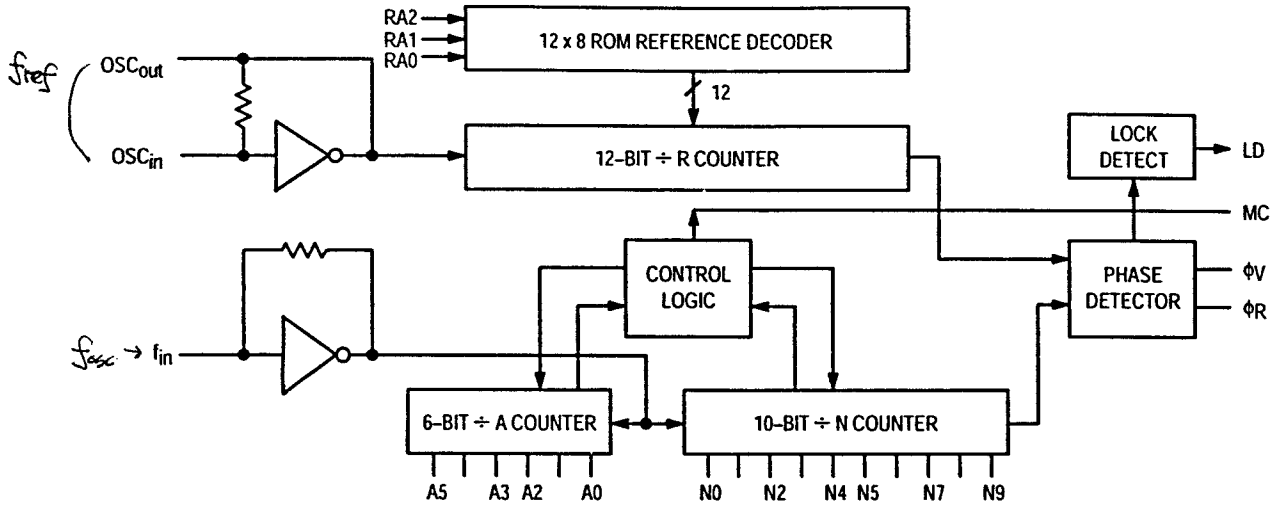
MC145152–2 BLOCK DIAGRAM



NOTE: N0 – N9, A0 – A5, and RA0 – RA2 have pull–up resistors that are not shown.

PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 1)

Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual–modulus prescaler and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0, RA1, RA2
Reference Address Inputs (Pins 4, 5, 6)

These three inputs establish a code defining one of eight possible divide values for the total reference divider. The total reference divide values are as follows:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

N0 – N9
N Counter Programming Inputs (Pins 11 – 20)

The N inputs provide the data that is preset into the ÷ N counter when it reaches the count of 0. N0 is the least significant digit and N9 is the most significant. Pull–up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

A0 – A5
A Counter Programming Inputs (Pins 23, 21, 22, 24, 25, 10)

The A inputs define the number of clock cycles of f_{in} that require a logic 0 on the MC output (see **Dual–Modulus Prescaling** section). The A inputs all have internal pull–up resistors that ensure that inputs left open will remain at a logic 1.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

φR, φV
Phase Detector B Outputs (Pins 7, 8) Active Low

These phase detector outputs can be combined externally for a loop–error signal.

If the frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by φV pulsing low. φR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by φR pulsing low. φV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both φV and φR remain high except for a small minimum time period when both pulse low in phase.

MC
Dual–Modulus Prescale Control Output (Pin 9)

Signal generated by the on–chip control logic circuitry for controlling an external dual–modulus prescaler. The MC level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first

portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low MC levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

LD
Lock Detector Output (Pin 28)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY

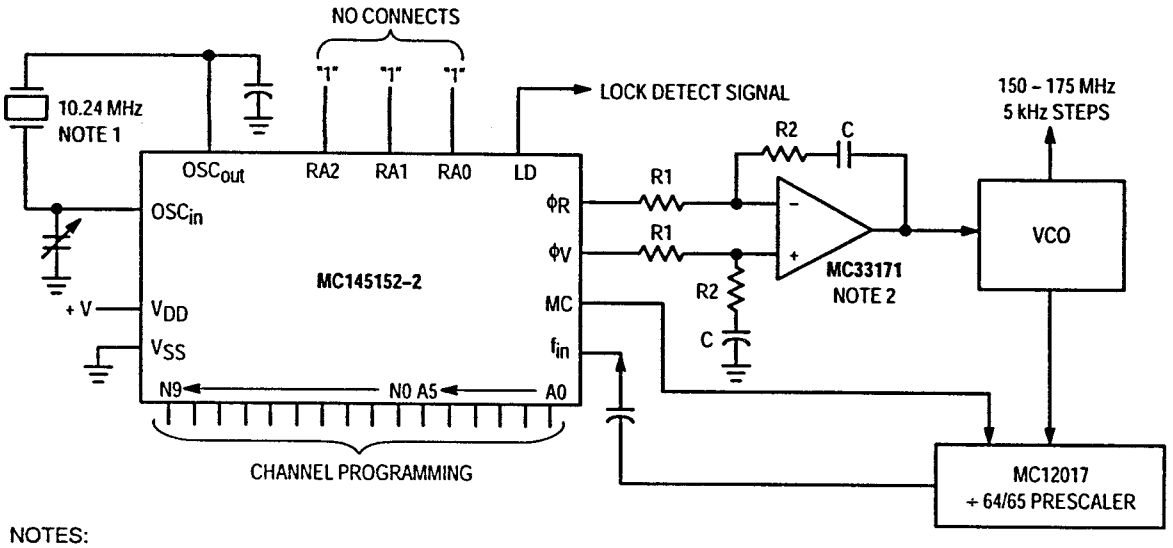
V_{DD}
Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 2)

The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



NOTES:
1. Off–chip oscillator optional.
2. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 1. Synthesizer for Land Mobile Radio VHF Bands

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct–coupled square wave having a rail–to–rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

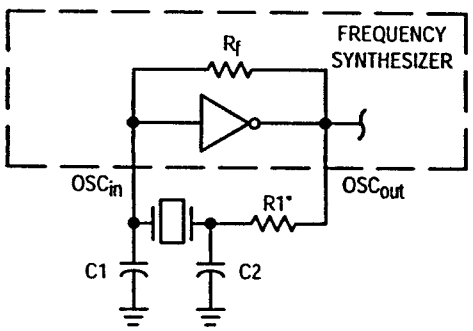
For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog*, the *Gold Book*, or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct–coupled square wave having rail–to–rail voltage swing.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 10.



* May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 11)
C_{out} = 6 pF (see Figure 11)
C_a = 1 pF (see Figure 11)
C_O = the crystal's holder capacitance (see Figure 12)
C1 and C2 = external capacitors (see Figure 10)

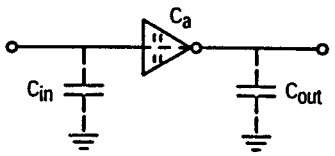
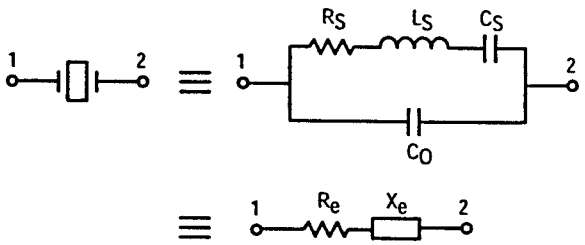


Figure 11. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure 10 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1 = 0 Ω).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 1).

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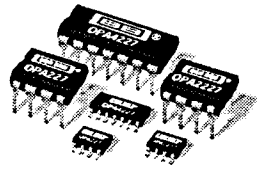

OPA227
OPA2227
OPA4227
OPA228
OPA2228
OPA4228

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High Precision, Low Noise OPERATIONAL AMPLIFIERS

FEATURES

- LOW NOISE: 3nV/√Hz
- WIDE BANDWIDTH:
  OPA227: 8MHz, 2.3V/µs
  OPA228: 33MHz, 10V/µs
- SETTLING TIME: 5µs
  (significant improvement over OP-27)
- HIGH CMRR: 138dB
- HIGH OPEN-LOOP GAIN: 160dB
- LOW INPUT BIAS CURRENT: 10nA max
- LOW OFFSET VOLTAGE: 75µV max
- WIDE SUPPLY RANGE: ±2.5V to ±18V
- OPA227 REPLACES OP-27, LT1007, MAX427
- OPA228 REPLACES OP-37, LT1037, MAX437
- SINGLE, DUAL, AND QUAD VERSIONS

APPLICATIONS

- DATA ACQUISITION
- TELECOM EQUIPMENT
- GEOPHYSICAL ANALYSIS
- VIBRATION ANALYSIS
- SPECTRAL ANALYSIS
- PROFESSIONAL AUDIO EQUIPMENT
- ACTIVE FILTERS
- POWER SUPPLY CONTROL

DESCRIPTION

The OPA227 and OPA228 series op amps combine low noise and wide bandwidth with high precision to make them the ideal choice for applications requiring both ac and precision dc performance.

The OPA227 is unity gain stable and features high slew rate (2.3V/µs) and wide bandwidth (8MHz). The OPA228 is optimized for closed-loop gains of 5 or greater, and offers higher speed with a slew rate of 10V/µs and a bandwidth of 33MHz.

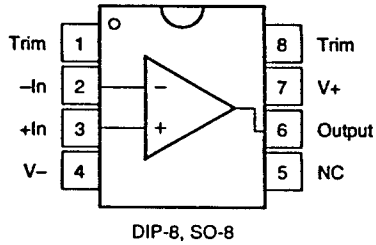
The OPA227 and OPA228 series op amps are ideal for professional audio equipment. In addition, low quiescent current and low cost make them ideal for portable applications requiring high precision.

The OPA227 and OPA228 series op amps are pin-for-pin replacements for the industry standard OP-27 and OP-37 with substantial improvements across the board. The dual and quad versions are available for space savings and per-channel cost reduction.

The OPA227, OPA228, OPA2227, and OPA2228 are available in DIP-8 and SO-8 packages. The OPA4227 and OPA4228 are available in DIP-14 and SO-14 packages with standard pin configurations. Operation is specified from –40°C to +85°C.

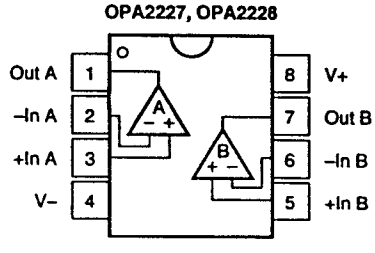
SPICE Model available for OPA227 at www.burr-brown.com

OPA227, OPA228



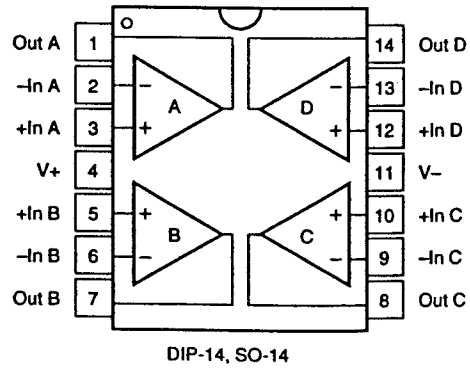
DIP-8, SO-8

OPA2227, OPA2228



DIP-8, SO-8

OPA4227, OPA4228



DIP-14, SO-14

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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PDS-1494B

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SPECIFICATIONS: V_S = ±5V to ±15V

OPA227 Series

At T_A = +25°C, and R_L = 10kΩ, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40°C to +85°C.

PARAMETER		CONDITION	OPA227P, U OPA2227P, U			OPA227PA, UA OPA2227PA, UA OPA4227PA, UA			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE									
Input Offset Voltage	V_{OS}			±5	±75		±10	±200	µV
T_A = –40°C to +85°C					**±100**			**±200**	µV
vs Temperature	dV_{OS}/dT			**±0.1**	**±0.6**		**±0.3**	**±2**	µV/°C
vs Power Supply	PSRR	V_S = ±2.5V to ±18V		±0.5	±2		*	*	µV/V
T_A = –40°C to +85°C					**±2**			*	µV/V
vs Time				0.2			*		µV/mo
Channel Separation (dual, quad)		dc		0.2			*		µV/V
		f = 1kHz, R_L = 5kΩ		110			*		dB
INPUT BIAS CURRENT									
Input Bias Current	I_B			±2.5	±10		*	*	nA
T_A = –40°C to +85°C					**±10**			*	nA
Input Offset Current	I_{OS}			±2.5	±10		*	*	nA
T_A = –40°C to +85°C					**±10**			*	nA
NOISE									
Input Voltage Noise, f = 0.1Hz to 10Hz				90			*		nVp-p
				15			*		nVrms
Input Voltage Noise Density, f = 10Hz	e_n			3.5			*		nV/√Hz
f = 100Hz				3			*		nV/√Hz
f = 1kHz				3			*		nV/√Hz
Current Noise Density, f = 1kHz	i_n			0.4			*		pA/√Hz
INPUT VOLTAGE RANGE									
Common-Mode Voltage Range	V_{CM}		(V–)+2		(V+)–2	*		*	V
Common-Mode Rejection	CMRR	V_{CM} = (V–)+2V to (V+)–2V	120	138		*	*		dB
T_A = –40°C to +85°C			**120**			*			dB
INPUT IMPEDANCE									
Differential				10^7 II 12			*		Ω II pF
Common-Mode		V_{CM} = (V–)+2V to (V+)–2V		10^9 II 3			*		Ω II pF
OPEN-LOOP GAIN									
Open-Loop Voltage Gain	A_{OL}	V_O = (V–)+2V to (V+)–2V, R_L = 10kΩ	132	160		*	*		dB
T_A = –40°C to +85°C			**132**			*			dB
		V_O = (V–)+3.5V to (V+)–3.5V, R_L = 600Ω	132	160		*	*		dB
T_A = –40°C to +85°C			**132**			*			dB
FREQUENCY RESPONSE									
Gain Bandwidth Product	GBW			8			*		MHz
Slew Rate	SR			2.3			*		V/µs
Settling Time: 0.1%		G = 1, 10V Step, C_L = 100pF		5			*		µs
0.01%		G = 1, 10V Step, C_L = 100pF		5.6			*		µs
Overload Recovery Time		V_{IN} • G = V_S		1.3			*		µs
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, G = 1, V_O = 3.5Vrms		0.00005			*		%
OUTPUT									
Voltage Output		R_L = 10kΩ	(V–)+2		(V+)–2	*		*	V
T_A = –40°C to +85°C		R_L = 10kΩ	**(V–)+2**		**(V+)–2**	*		*	V
		R_L = 600Ω	(V–)+3.5		(V+)–3.5	*		*	V
T_A = –40°C to +85°C		R_L = 600Ω	**(V–)+3.5**		**(V+)–3.5**	*		*	V
Short-Circuit Current	I_{SC}			±45			*		mA
Capacitive Load Drive	C_{LOAD}			See Typical Curve			*		
POWER SUPPLY									
Specified Voltage Range	V_S		±5		±15	*		*	V
Operating Voltage Range			±2.5		±18	*		*	V
Quiescent Current (per amplifier)	I_Q	I_O = 0		±3.7	±3.8		*	*	mA
T_A = –40°C to +85°C		I_O = 0			**±4.2**			*	mA
TEMPERATURE RANCE									
Specified Range			–40		+85	*		*	°C
Operating Range			–55		+125	*		*	°C
Storage Range			–65		+150	*		*	°C
Thermal Resistance	θ_{JA}								
SO-8 Surface Mount				150			*		°C/W
DIP-8				100			*		°C/W
DIP-14				80			*		°C/W
SO-14 Surface Mount				100			*		°C/W

* Specifications same as OPA227P, U.

WIRELESS RADIO™ OSCILLATORS

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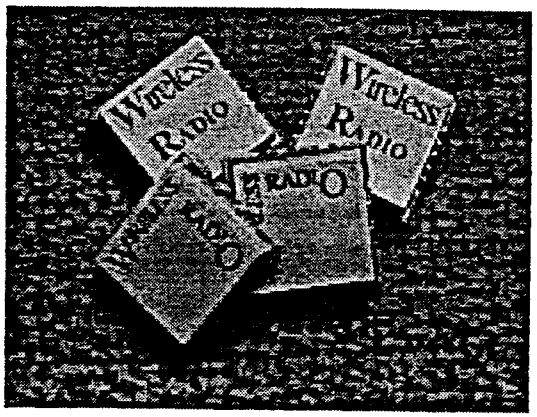
On-Line WebPage Catalog

Surface Mount Voltage Controlled Oscillator
VCO V2-1140 1050-1875 MHz

Features

- Surface Mount / Tape & Reel
- Small .50 in. x .50 in. x .10 in. size
- Linear Wideband Tuning Range
- Low Cost



Description

The VCO V2-1140 is a fundamental mode reflection oscillator that utilizes a silicon bipolar transistor and hyper-abrupt silicon varactor diodes to create a highly linear VCO with wideband tuning characteristics. The device is useful for many wireless applications where high frequency and linear modulation is required.

The device is very repeatable from unit to unit and assembled in ISO 9000 qualified manufacturing facility with the latest surface mount equipment. Every unit is DC and RF tested with our fully automated computerized test stands to provide the highest reliability and guaranteed performance.

Absolute Maximum Ratings

Parameter	Maximum
Supply Voltage	+15V
Tuning Voltage	+22V
Storage Temp.	-45C to +95C
Operating Temp.	-40C to +85C

Electrical Specifications

Parameter	Test Condition	Units	Min	Typ	Max
Frequency Range	1140 - 1875	MHz	1140		1875
Tuning Voltage	Vt	V	0		+10
RF Output Power	1140-1875 MHz	dBm		+8	
Supply Voltage	Vcc	V		+10	
Supply Current	Icc	mA		26	
Phase Noise	ssb @100 KHz	dBc/Hz		-112	
Modulation Sensitivity	Vt=1-10v	MHz/V		70	
Tuning Linearity		ratio		1.3	2.1
Modulation BW	3 dB BW	MHz		20	
Harmonics	2nd	dBc		-12	
Frequency Pushing	Vcc=9.75 - 10.25	MHz/V			3
Frequency Pulling	1.5:1 VSWR	MHz			5
Frequency Drift	0 to +85 C	MHz/C			6
Tuning Input Capacitance		pF		27	

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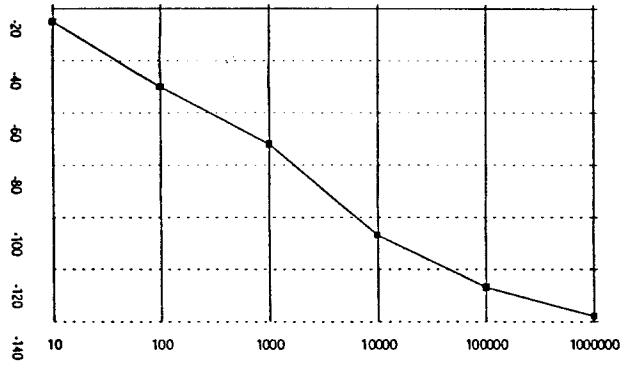
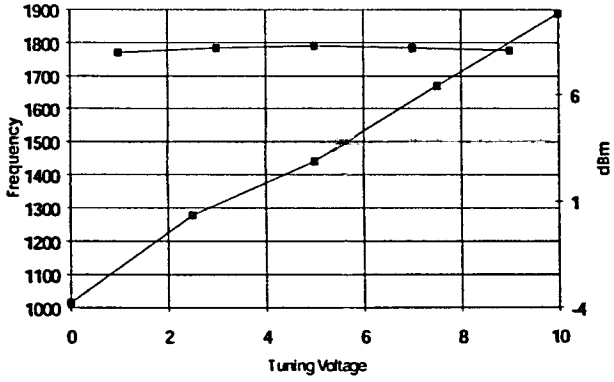
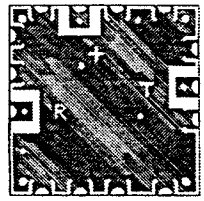
Typical Performance @ +25 C

Phase Noise

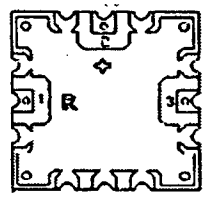


Freq. vs. Tuning V.

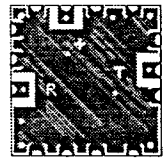




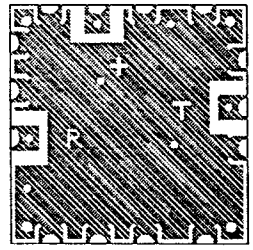
mini-Z pkg .50 x .50 x .20
(shown X2 actual size).
Bottom View



SM pkg .50 x .50 x .20
(shown X2 actual size).
Bottom View



SUB pkg .375 x .375 x .11
(shown X2 actual size).
Bottom View



S pkg .91 x .91 x .25
(shown X1.5 actual size)
Bottom View

1) Exceeding limits may cause permanent damage.
2) External bypassing of both Vcc and Vt can improve phase noise performance and power supply decoupling.
3) This device is designed to operate over 0 to +70 C.

Wireless Radio, POB 452, Dexter, MI 48130

www.wireless-radio.com

Specifications subject to change without notice.

Order this document by MC12054A/D

MOTOROLA

2.0 GHz Super Low Power Dual Modulus Prescaler

The MC12054A is a super low power dual modulus prescaler used in phase-locked loop applications. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 5.4 mW at a minimum supply voltage of 2.7 V.

The MC12054A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 2.0 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0 GHz Toggle Frequency
- The MC12054 is Pin and Functionally Compatible with the MC12031
- Low Power 2.0 mA Typical
- 2.6mA Maximum, –40 to 85°C, V_{CC} = 2.7 to 5.5 Vdc
- Short Setup Time (t_{set}) 10ns Maximum @ 2.0 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Maximum Input Voltage Should Be Limited to 6.5 Vdc

MOSAIC V is a trademark of Motorola

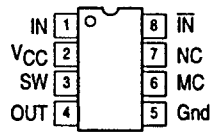
MC12054A

MECL PLL COMPONENTS
÷64/65, ÷128/129 LOW POWER DUAL MODULUS PRESCALER

SEMICONDUCTOR TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 7.0	Vdc
Operating Temperature Range	T_A	–40 to 85	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc

NOTE: ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC12054AD	T_A = –40 to 85°C	SO–8

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ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 Vdc, T_A = –40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	2.5	2.0	GHz
Supply Current (Pin 2)	I_{CC}	–	2.0	2.6	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	V_{CC} + 0.5 V	V
Modulus Control Input Low (MC)	V_{IL1}	Gnd	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	V_{CC} – 0.5 V	V_{CC}	V_{CC} + 0.5 V	VDC
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	–
Output Voltage Swing (Note 2) (C_L = 8.0 pF, R_L = 1.65 kΩ)	V_{out}	0.8	1.1	–	V_{pp}
Modulus Setup Time MC to Out @ 2000 MHz	t_{set}	–	8.0	10	ns
Input Voltage Sensitivity 250–2000 MHz 100–250 MHz	V_{in}	100 400	– –	1000 1000	mVpp
Output Current (Note 1) V_{CC} = 2.7 V, C_L = 8.0 pF, R_L = 1.65 kΩ V_{CC} = 5.0 V, C_L = 8.0 pF, R_L = 3.6 kΩ	I_O	 – –	 1.0 1.0	 4.0 4.0	mA

NOTES: 1. Divide ratio of +64/65 @ 2.0 GHz
2. Valid over voltage range 2.7 to 5.5 V; R_L = 1.65 kΩ @ V_{CC} = 2.7 V; R_L = 3.6 kΩ @ V_{CC} = 5.0 V

Figure 1. Logic Diagram (MC12054A)

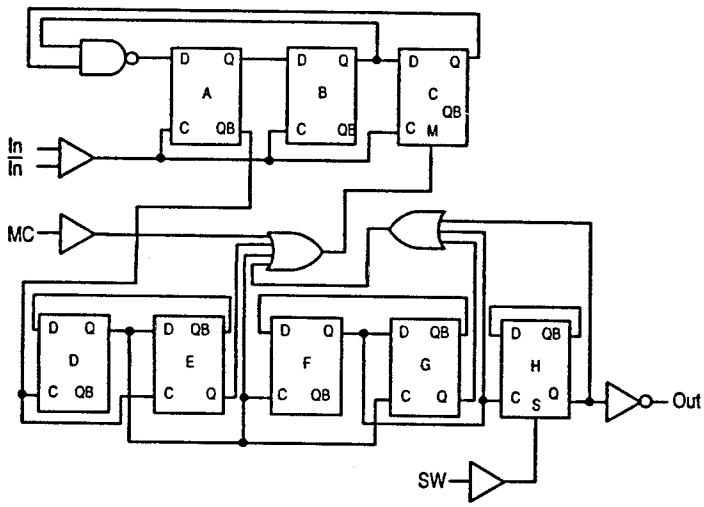
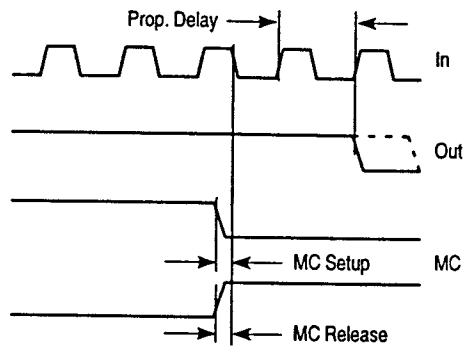
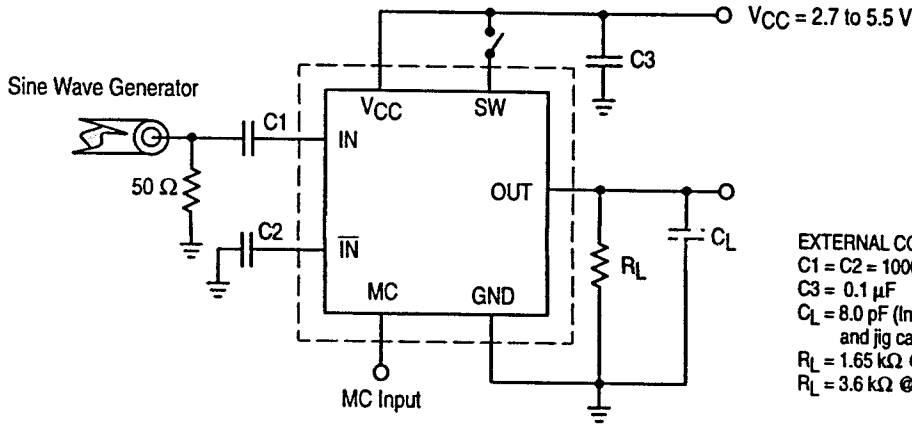


Figure 2. Modulus Setup Time



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. AC Test Circuit



EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 µF
C_L = 8.0 pF (Including Scope and jig capacitance)
R_L = 1.65 kΩ @ V_{CC} = 2.7 V
R_L = 3.6 kΩ @ V_{CC} = 5.0 V