REVIEW FOR FINAL EXAMINATION

The final examination will be held on Monday, July 28, 2003 from 2:50pm to 5:40pm in Room C341of Van Leer. The exam is open lecture notes only (notes from L010 through L220). The exam will consist of 7 problems of which 5 problems, each worth 20 points for a total of 100 points, must be worked. The 7 problems will fall into two categories, those you must work and those you may work. Below is a list of the material for which you are responsible. Basically, the final will be cover all of the lecture notes plus the accompanying homework problems with the exception of L190.

Introduction to Frequency Synthesizers

Characterization of frequency synthesizers
Types of frequency synthesizers
- Incoherent synthesis
- Coherent direct synthesis
- Cohernet direct digital synthesis
- Coherent indirect synthesis

Frequency translation
Filters

Discrete and Integrated Circuit Technology

Discrete components
- Passive components – definition and characteristics, types, range of values, variable components

Integrated components
- Characteristics of a modern technology
- Passive elements compatible with IC technology – characteristics, range of values

LPLL and DPLLs

Phase detectors - Multipliers, EXOR, JK, PFD
Filters – Passive, active, charge pump
Locked relationships
Open loop – phase margin, crossover frequency
Closed loop – transfer functions in the frequency domain for various stimulations (phase step, frequency step, frequency ramp)
Steady-state phase error
Unlocked state – acquisition process
- Hold, Pull-In, Pull-Out, and Lock ranges and times

Noise relationships
LPLL and DPLL design

ADPLLs

General concepts only

PLL Design Equations and Relationships

Type and order of the loop
Be able to develop the design equations given a different configuration
Know the design equations for Type I, first- and second-order loops and for Type II, second-order loop

Applications of Frequency Synthesizers

Modulation – amplitude, frequency and phase
SSB spurs
Noise in PLLs – VCO, reference
Use of the PLL for modulation and demodulation

Frequency synthesizers-
- Multi-loop
- Fractional-N

PLL Circuits

Analog multiplier circuits
Digital detector circuits
Filters
Charge pumps
Voltage controlled oscillators
- Tuned – RC, LC
- Untuned – Relaxation,
- Frequency of oscillation
- Gain of the loop
- Amplitude stabilization principle
- Varactors

Phase Noise

Jitter and phase noise in PLLs
Spurious sidebands in PLLs (phase detector)
Linear time invarient model of VCO phase noise
Linear time varying model of VCO phase noise
Phase noise in LC oscillators
Phase noise in ring oscillators

Ring Oscillators

Basic theory
Tuning
Noise principles applied to ring oscillators
Multiple-pass loop architectures

Frequency Synthesizers

Applications of PLLs – demodulation and modulation, signal conditioning frequency synthesis, clock and data recovery, frequency translation
Integrated circuit frequency synthesizers – components, architectures
Dividers for frequency synthesizers
- Fixed
- Dual Modulus
- Programmable
- Delta-Sigma techniques

GSM example of an integrated circuit frequency synthesizer
All digital frequency synthesizer for Bluetooth applications

Clock and Data Recovery Circuits

NRZ data and basics of CDR circuits
Phase and frequency detectors for random data
CDR architectures
VCOs for CDR applications
Examples of CDR circuits