FINAL EXAMINATION

NAME_____SCORE_____/100

Problem	①	②	3	4	5	6	7	Sum
Points								

INSTRUCTIONS: This exam is open lecture notes only (L010 through L220 excluding L190). The exam consists of 7, 20-point problems of which you are to work only 5 for a total of 100 points. Problems 1 and 2 must be worked and you may choose any three of the last six problems for a total of five problems. Please circle the number in the table above of the five problems you wish graded. If you do not indicate the problems to be graded, then problems 1 through 5 will be graded regardless of whether they are worked or not. Be sure to turn in only the 5 problems you wish graded in proper numerical order. Please show your work leading to your answers so that maximum partial credit may be given where appropriate.

Problem 1 - (20 points – This problem must be attempted)

A DPLL frequency synthesizer has the following parameters:

$F(s) = \frac{1+0.01s}{s}$ $K_o = 2\text{x}10^6$ (rads/V) $K_d = 0.8$V/rad

$\beta = 2\pi$ $N = 150$ $f_{ref} = 120$ kHz

The temperature is 290°K and all circuits operate from a ±5V power supply.

(a.) What is the output frequency hold range in Hz?

(b.) What is the output frequency lock (capture) range in Hz? What is the lock (capture) time in seconds? (Note that K in the L090-2 notes is K_oK_d/N and not $K_oK_dF(0)/N$).

(c.) Assume that you wish to phase modulate the output of the synthesizer, where would you introduce the modulating voltage? What is the peak amplitude of the 1 kHz ac signal needed to produce an output peak phase deviation of 0.5 radians?

Problem 2 - (20 points – This problem must be attempted)

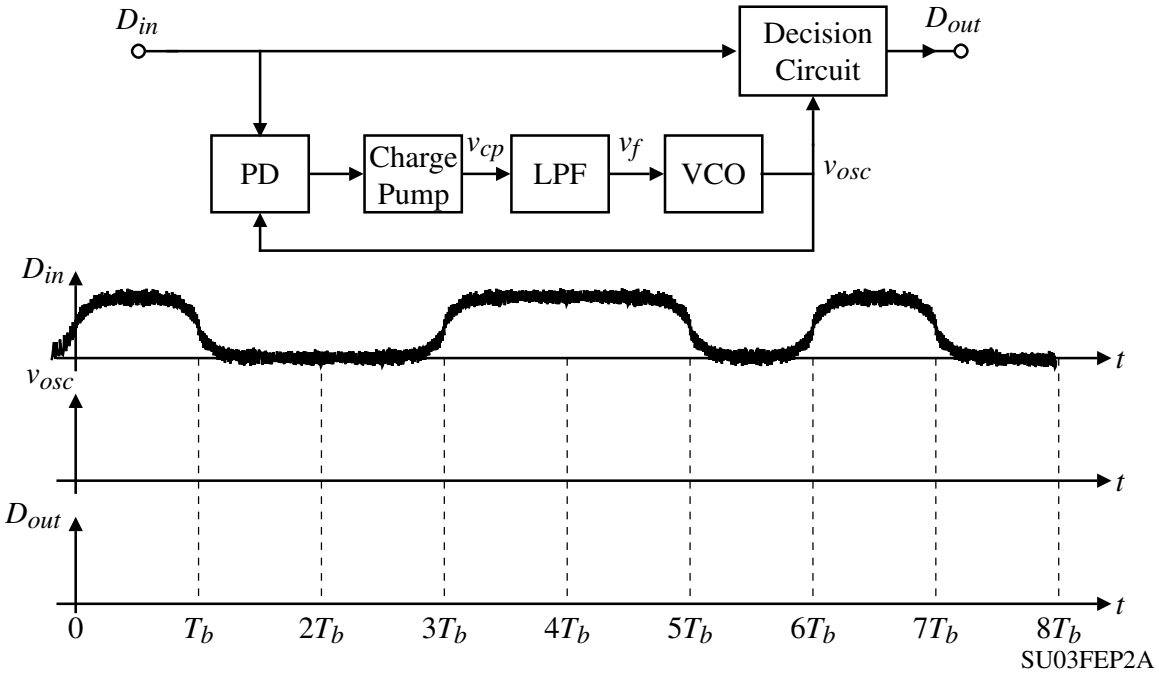
(a.) What is non-return-to-zero (NRZ) data and why is it preferable over return-to-zero (RZ) data?

(b.) What is the differences between a linear and a bang-bang phase detector for clock and data recovery (CDR) applications?

(c.) What are the sources of jitter in a CDR?

(d.) What is a half-rate phase detector? How does it work?

(e.) Sketch the approximate waveforms for optimum performance for the CDR circuit shown on the plots given.



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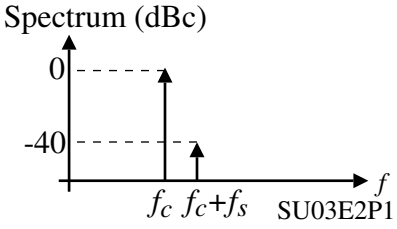
Problem 3 - (20 points – This problem is optional)

A carrier together with a single –40dBc spur 1kHz above the carrier are applied to an ideal limiter. Sketch the spectrum of the output of the limiter considering frequencies through the 5th harmonic of the carrier. Assume the limiter acts like a square wave modulator resulting in odd harmonics only whose amplitudes are given as $a_n = (4/n\pi)$ where n = the harmonic.

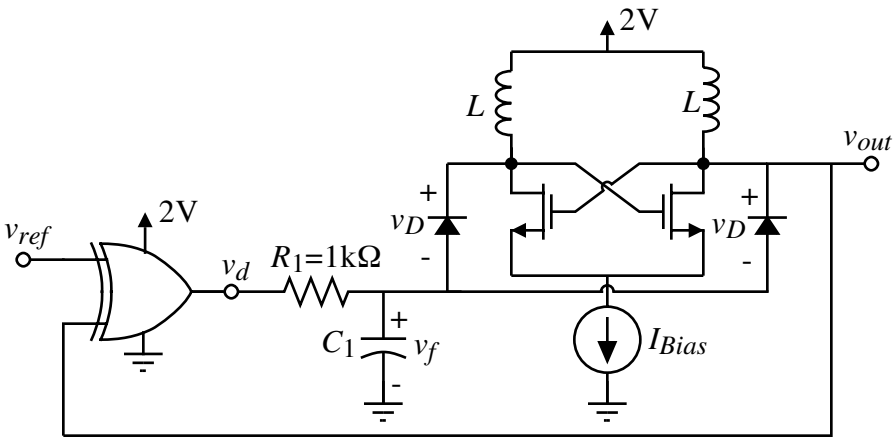


Problem 4 - (20 points – This problem is optional)

A simple implementation of a CMOS PLL is shown. The phase detector output is fed to a first-order lowpass filter whose output changes the varactor capacitance to change the VCO frequency. If the VCO frequency is 500 MHz and the varactor capacitance varies as

$$C = \frac{C_o}{\sqrt{1+v_D}}$$

what value of C_1 will give a phase margin of 45° if $v_f \approx 1$V? If you need to make any assumptions in working this problem, make sure they are clearly stated.



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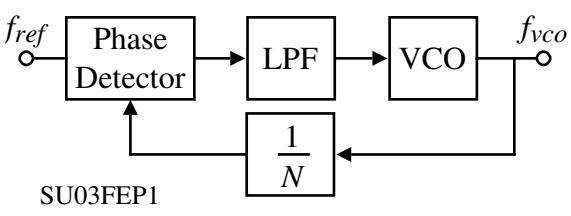
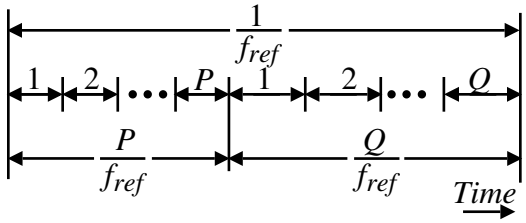
Problem 5 – (20 points – This problem is optional)

The block diagram for a fractional-N frequency synthesizer is shown. The effective N is normally given as shown below (see page 100-30 of the lecture notes) where the divider divides by N_1 for P cycles (periods) and N_2 for Q cycles (periods).

$$N_{eff} = \frac{PN_1 + QN_2}{P+Q}$$

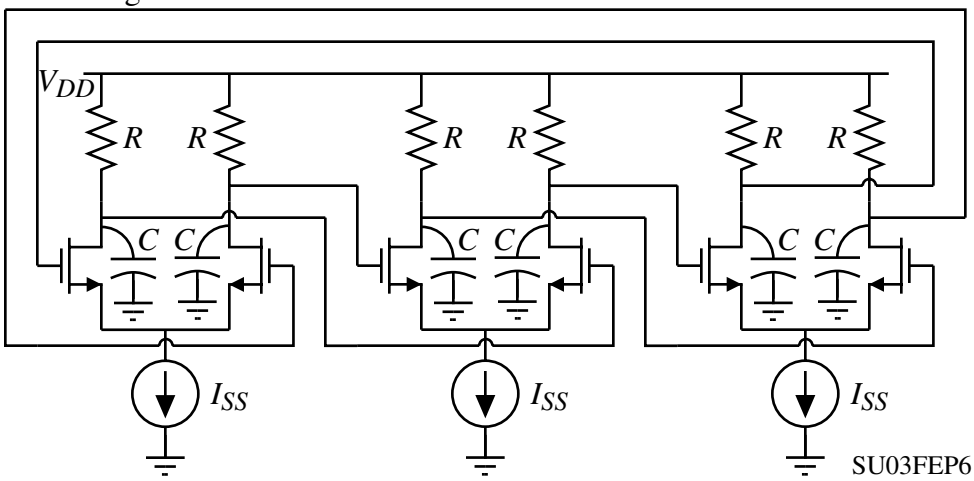
The above relationship is only good when N_{eff} is large. (a.) Derive a better expression for N_{eff} based on the diagram shown which takes into account that f_{ref} always remains constant but that the output frequency of the VCO, f_{VCO}, changes as N changes. (b.) If $P = 1$, $Q = M-1$, $N_1 = N+1$ and $N_2 = N$, find N_{eff} for both the above expression and the one derived in (a.). (c.) If $M = 100$ and $N = 1000$, what is the effective N for both expressions?





Problem 6 – (20 points – This problem is optional)

A differential ring oscillator is shown.



(a.) Find the frequency of oscillation in Hz if R = 1kΩ and C = 1pF.

(b.) What value of g_m is required for oscillation assuming all stages are identical?

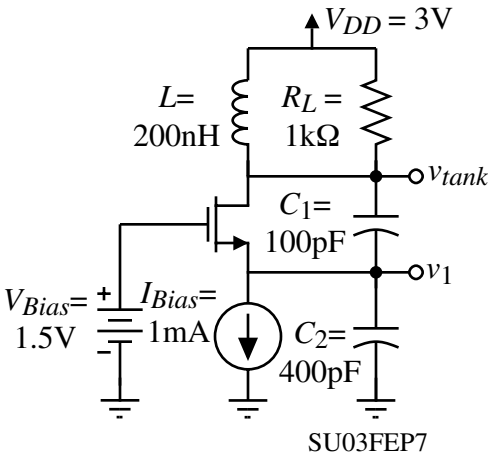
(c.) What is the maximum positive and maximum negative voltage swing at the drains if I_{SS} = 1mA and V_{DD} = 2V?

Problem 7 – (20 points – This problem is optional)

An LC oscillator is shown (a.) What is the frequency of oscillation of this oscillator? (b.) At room temperature, assume that the noise of R_L is dominant over all other noise sources and calculate the single sideband phase noise resulting from the resistor's noise using the linear time varying theory if $\Gamma_{rms}^2 = 0.5$. Note that the tank voltage, v_{tank} can be approximated as

$$v_{tank} \approx 2I_{Bias}R_L\left(1 - \frac{C_1}{C_1+C_2}\right)$$

(c.) At an offset of 200kHz, what is the phase noise in dBc?



Extra Sheet