Homework Assignment No. 2

This homework assignment is due in class on Wednesday, May 28, 2003.

Problem 1 - (10 points)

A phase-locked loop has a center frequency of 10^5 rads/s, a K_o of 10^3 rad/V-s, and a K_d of 1 V/rad. Assume there is no other gain in the loop. Determine the loop bandwidth in the first-order loop configuration. Determine the single-pole, loop-filter pole location to give the closed-loop poles located on 45° radials from the origin of the complex frequency plane.

Problem 2 – (10 points)

For the same PLL of the previous problem, design a loop filter with a zero that gives a crossover frequency for the loop gain of 100 rads/sec. The loop phase shift at the loop crossover frequency should be –135°.

Problem 3 – (10 points)

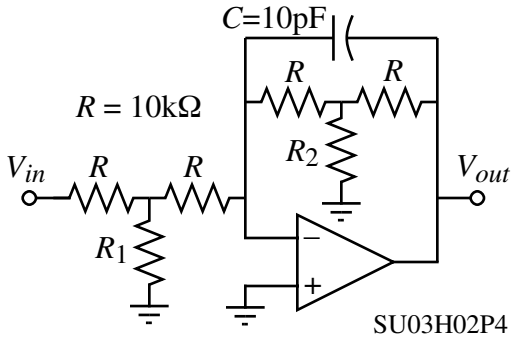
Estimate the capture range of the PLL of the previous problem assuming that it is not artificially limited by the VCO frequency range.

Problem 4 – (10 points)

A filter for a phase locked loop is specified as

$$|F(s)| = \frac{\omega_1}{s+\omega_1} = \frac{1{,}000{,}000}{s+100{,}000}$$

and must be implemented on a CMOS chip using resistors no larger than 10kΩ and capacitors no larger than 10pF. Using the circuit shown, find the values of R_1 and R_2 that will satisfy the component value constraints.



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Problem 5 – (20 points)

This homework is designed to provide practical inductor design experience for students. Use ASITIC for the design and analysis. However, other tools are acceptable if they give all the results including layout. See lecture 045 on Monolithic Inductor Design in Silicon Technology)

A 5GHz LC tank will be designed as a part of LC oscillator. C value is given as 1pF.

(a) Find L value. (b) Design and simulate a spiral inductor with this L value (± 5% range). Optimize design parameters, W, S, D and N to get a high Q (Q_{min} = 5). Show L, Q, f_{SR} value obtained from simulation. (c) Show the layout. (d) Give a lumped circuit model with component values.