MONOLITHIC INDUCTOR DESIGN IN SI TECHNOLOGY

Objective

The objective of this presentation is:

1.) Illustrate the design and analysis of on-chip spiral inductor.

2.) Show an inductor design example using ASITIC.

Outline

- Spiral Inductors
- Inductor Modeling
- Design Guidelines for CMOS Spiral Inductors
- ASITIC overview
- Design Example
- References

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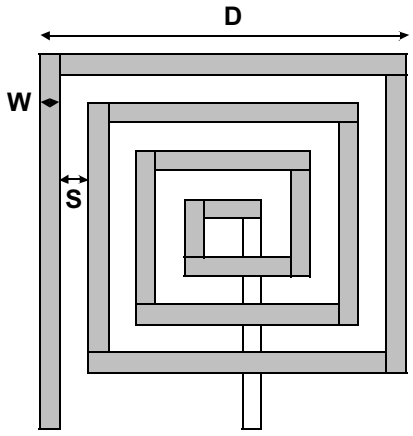
Spiral Inductors

The most widely used on-chip inductor is a spiral inductor.



D: diameter
W: width of a spiral
S: spacing between turns
N: number of turns

- Design Parameters
  - Diameter, D, is mainly decided from area restriction.
  - Remaining parameters, W, S, and N are optimized to get
    - **i)** Desired inductance value, L
    - **ii)** High quality factor, Q
    - **iii)** High self-resonant frequency, f_{SR}

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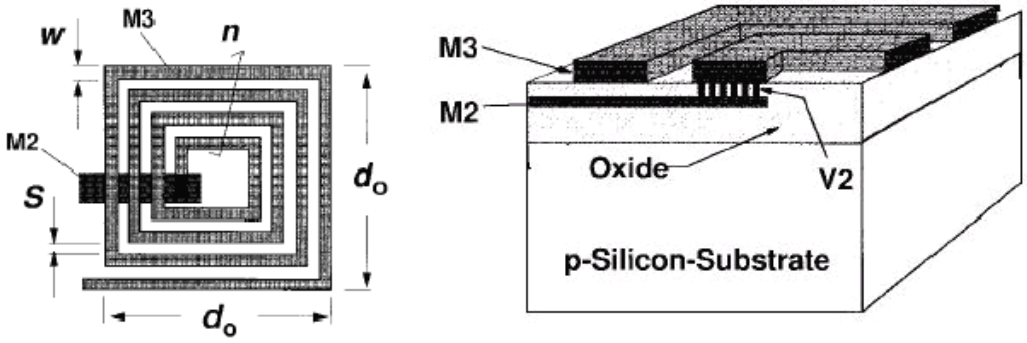
Spiral Inductors

- Implementation
  - Spiral inductor is implemented using metal layers in Si technology.
  - Topmost metal is preferred because of its low resistivity.
  - More than one metal layers can be connected together to reduce resistance or area.
  - The accurate analysis of a spiral inductor requires complex electro-magnetic simulation.



(a) (b)

(a) top view (b)cross-sectional view of a spiral inductor using three metal process [3]

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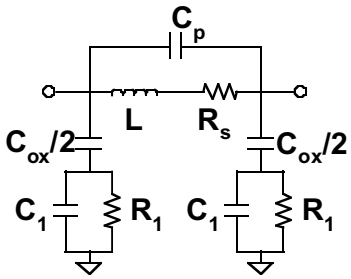
Inductor Modeling

A lumped circuit model can be developed to show spiral inductor conceptually and to be used in circuit design.



$$L \approx \frac{37.5\mu_0 N^2 a^2}{11D - 14a}$$

$$R_S \approx \frac{l}{W \cdot \sigma \cdot \delta(1 - e^{-t/\delta})}$$

$$C_P = N \cdot W^2 \cdot \frac{\varepsilon_{ox}}{t_{ox}}$$

$$C_{ox} = W \cdot L \cdot \frac{\varepsilon_{ox}}{t_{ox}}$$

$$R_1 \approx \frac{2}{W \cdot L \cdot G_{sub}}$$

$$C_1 \approx \frac{W \cdot L \cdot C_{sub}}{2}$$

where

$\mu_0 = 4\pi \times 10^{-7}$, σ is the conductivity of the material

a is the distance from the center of the inductor to the middle of the windings

L is the total length of the spiral, t is the thickness of the metal,

δ is the skin depth given by $\delta = \sqrt{\frac{2}{W\mu_0\sigma}}$, $G_{sub}(C_{sub})$ is process-dependent parameters.

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Inductor Modeling

- Components
  - R_s: low-frequency resistive loss of a metal and skin effect.
  - C_p: arises from the overlap of the cross-under with the rest of the spiral. The lateral capacitance from turn to turn is included.
  - C_{ox}: capacitance between the spiral and the substrate
  - R_1: substrate loss
  - C_1: capacitance of the substrate
- Design specifications
  - L: desired inductance value
  - Q: quality factor. Simple approximation is

$$Q = \frac{\omega L}{R_S}$$

  - f_{SR} : self-resonant frequency. The resonant frequency of LC combination represents the upper useful frequency limit of the inductor. Inductor operation frequency should be lower than f_{SR}, $f < f_{SR}$

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Design Guidelines for CMOS Spiral Inductors [4]

- D: outer diameter
  - D↑ - Q↑ for small D, but self-resonant frequency, f_{SR}↓, as parasitic capacitance between the substrate and the spiral increases.
  - A good design usually has D < 200μm.

- W: metal width
  - Metal width should be as wide as possible.
  - W↑ - Q↑ as R_s↓
  - However, as W > Wopt, skin effects appear in metal traces, increasing R_s.
  - A good design uses 10μm < W < 20μm.

- S: spacing between turns
  - Spacing should be as small as possible.
  - S↑ - L↑ as M (mutual inductance)↓
  - Use minimum metal spacing allowed in the technology (ex., $S_{min} \approx$ 1~5um in CMOS). Make sure the inter-winding capacitance between turns is not significant.

- N: number of turns
  - Use a value that gives a layout convenient to work with other parts of circuits.

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ASITIC

• Overview
- An analysis and simulation tool for spiral inductors and transformers for ICs
- Developed by Ali M. Niknejad at UC Berkeley
- Document: http://formosa.eecs.berkeley.edu/~niknejad/asitic.html

• Procedure
- Log on to UNIX account.
- Make a directory for ASITIC files (ex. 'my_asitic')
- Copy a technology file (CMOS.tek) to working directory. This is the default tech file that can be replaced for other processes.
  > cp /a/yamsrv1.ece.gatech.edu/export/home3/asitic/common/tek/CMOS.tek .
- Start ASITIC program with following command
  > /a/yamsrv1.ece.gatech.edu/export/home3/asitic/asitic_sun -8 -t CMOS.tek
- ASITIC window will pop up and command line shows a prompt for the program. ASITIC>
- Create, analyze and optimize inductors using commands.
- Useful command: sq, optl, pix and etc. For reference, refer 'Command Reference' section of the documentation.

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Design Example

A 2GHz LC tank will be designed as a part of LC oscillator. C value is given as 3pF.

(a) Find L value. (b) Design a spiral inductor with L value (± 5% range) from (a) using ASITIC. Optimize design parameters, W, S, D and N to get a high Q ($Q_{min} = 5$). Show L, Q, f_{SR} value obtained from simulation. (c) Show the layout. (d) Give a lumped circuit model.

Solution

(a) LC tank oscillation frequency is given as 2GHz.

$$\omega_{osc} = \frac{1}{\sqrt{LC}}, \quad L = \frac{1}{\omega_{osc}^2 \cdot C} = \frac{1}{(2\pi \cdot 2\times 10^9)^2 \cdot (3\times 10^{-12})} = 2.11\times 10^{-9}$$

L = 2.11nH is desired.

(b) L = 2.11nH(± 5%) is used as input parameter. Several design parameters are tried to get high Q and f_{SR} values. Final design has
- Parameters: W = 19um, S = 1um, D = 200um, N =3 .5
- Resulting inductor: L = 2.06nH, Q = 7.11, f_{SR} = 9.99GHz @ 2GHz

This design is acceptable as $Q > Q_{min}$ and $f < f_{SR}$.

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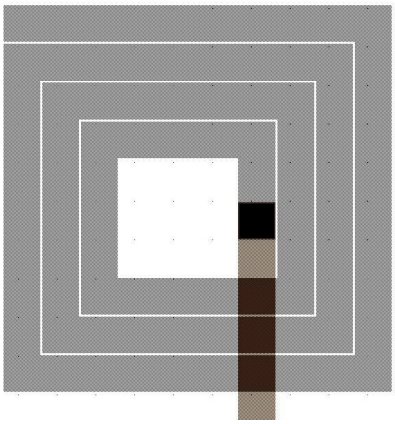
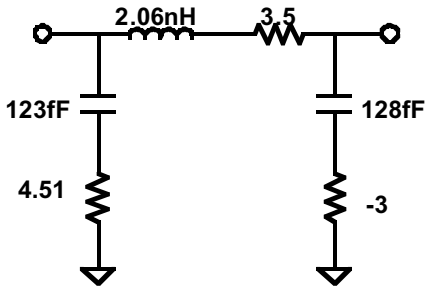
Design Example

(c) ASITIC generates a layout automatically. It can be saved and imported to use in other tools such as Cadence, ADS and Sonnet.



(d) Analysis in ASITIC gives a pi model.



Pi model is usually not symmetrical and this can be used for differential configuration where none of the two ports is ac-grounded.

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References

[1] Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge

[2] Behzad Razavi, *Design of Integrated Circuits for Optical Communications*, McGraw Hill

[3] Joachim N. Burghartz and et al, "RF Circuit Design Aspects of Spiral Inductors on Silicon", *IEEE J. Solid-State Circuits*, vol. 33, no.12, pp. 2028-2034,1998

[4] Jaime Aguilera and et al, "A Guide for On-Chip Inductor Design in a Conventional CMOS Process for RF Applications", *Applied Microwave & Wireless*, pp. 56-65, October 2001

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