LECTURE 170 – APPLICATIONS OF PLLS AND FREQUENCY DIVIDERS (PRESCALERS)

(References [2, 3, 4, 6, 11])

Objective

The objective of this presentation is:

1.) Examine the applications of PLLs

2.) Develop and characterize the techniques used for frequency division

Outline

- Applications of PLLs
- Integrated Circuit Frequency Synthesizers – Architectures and Techniques
- Dividers for Frequency Synthesizers
- Noise-Shaping Techniques
- Summary

APPLICATIONS OF PLLS

The PLL

The PLL is a very versatile building block and is suitable for a variety of applications including:

1.) Demodulation and modulation

2.) Signal conditioning

3.) Frequency synthesis

4.) Clock and data recovery

5.) Frequency translation

FM Demodulation

When the PLL is locked on a frequency modulated signal, the controlling voltage to the VCO becomes proportional to the frequency.

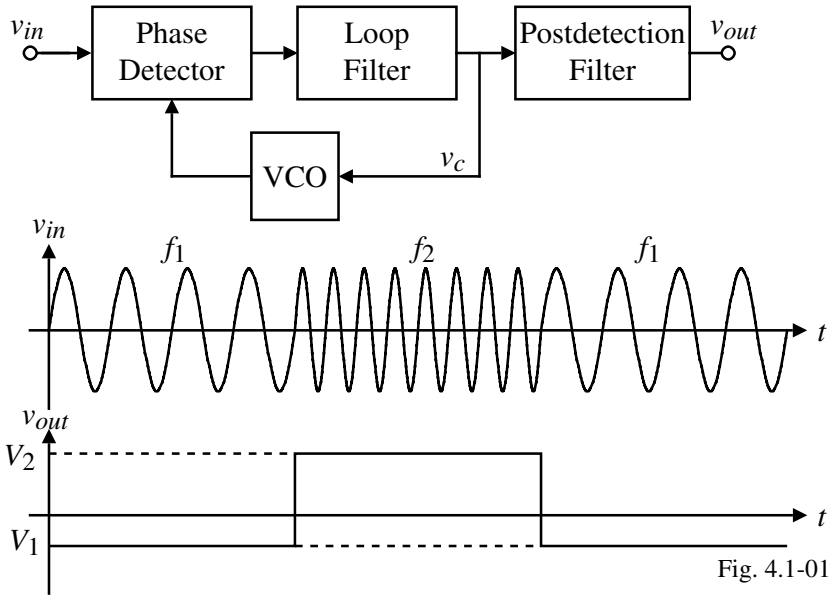


Fig. 4.1-01

Can be used for frequency shift keying (FSK) if a voltage discriminator is placed at the output.

FM Demodulation – Example

If $K_O = 2\pi(1\text{kHz/Volt})$, $K_V = 500$ (sec^{-1}) and $\omega_o = 1000\pi$ rads/sec ($f_o = 500$Hz) for the FM demodulator on the previous slide,

(a.) Find V_o for $f_i = 250$Hz and 1000Hz.

(b.) What is the time constant of V_o for a step change between these two frequencies?

Solution

(a.) We know that

$$\omega_{osc} = \omega_i = \omega_o + K_O V_O \qquad \rightarrow \qquad V_O = \frac{\omega_i - \omega_o}{K_O}$$

$$\therefore \qquad V_O(250\text{Hz}) = \frac{250-500}{1000} = -0.25\text{V}$$

$$V_O(1000\text{Hz}) = \frac{1000-500}{1000} = +0.5\text{V}$$

(b.) $\tau = \dfrac{1}{K_V} = 2\text{ms}$

We note that the risetimes of the square wave on the previous page would no longer be zero but take about 10ms to go from one level to another.

FM Demodulator – Example –Continued

Example:

For the PLL of the previous example, find $v_o(t)$ if the input signal is frequency modulated so that

$$\omega_i(t) = 2\pi(500\text{Hz})[1+0.1\sin(2\pi\text{x}10^2)t].$$

Solution

$$\frac{V_o(j\omega)}{\omega_i(j\omega)} = \frac{1}{K_o}\left(\frac{K_v}{K_v + j\omega}\right) = \frac{1}{K_o}\left(\frac{K_v}{K_v + \text{j}2\pi\text{x}100}\right)\Bigg|_{\omega=200\pi}$$

$$= \frac{1}{2000\pi}\left(\frac{500}{500+\text{j}628}\right) = \frac{1}{2000\pi}(0.39\text{-j}0.48)$$

$$|\omega_i(j\omega)| = 0.1(1000\pi) = 100\pi = 50(2\pi)$$

$$\therefore \quad V_o(j\omega) = \frac{50}{1000}(0.39\text{-j}0.48) = \frac{50}{1000}\,0.62\underline{/-51°} = 0.031\underline{/-51°}$$

or

$$v_o(t) = 0.031\,\sin[(2\pi\text{x}10^2)-51°]$$

Phase Modulator

When the PLL is locked on a fixed frequency, a slowly varying signal, $v_m(t)$, can be used to cause the phase shift of the *VCO* to shift achieving a phase modulator.

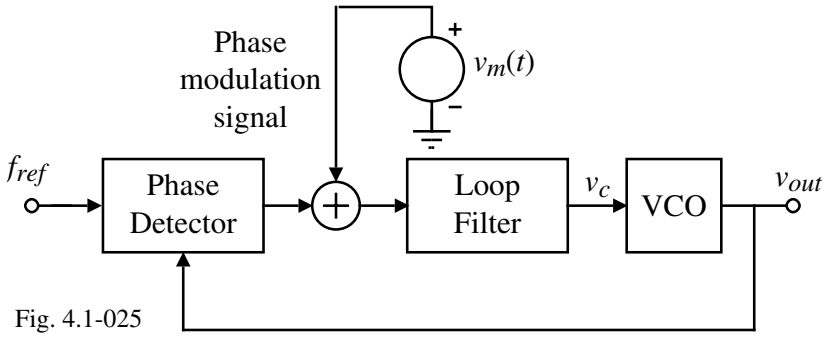


Fig. 4.1-025

$$v_{out}(t) = V_{out}\cos[\omega_{ref}t + \theta_m(t)]$$

where

$$\theta_m(t) = \frac{1}{K_d}v_m(t)$$

Signal Conditioning

The PLL can operate as a narrowband filter with an extremely high Q to select a desired signal in the presence of undesired signals.

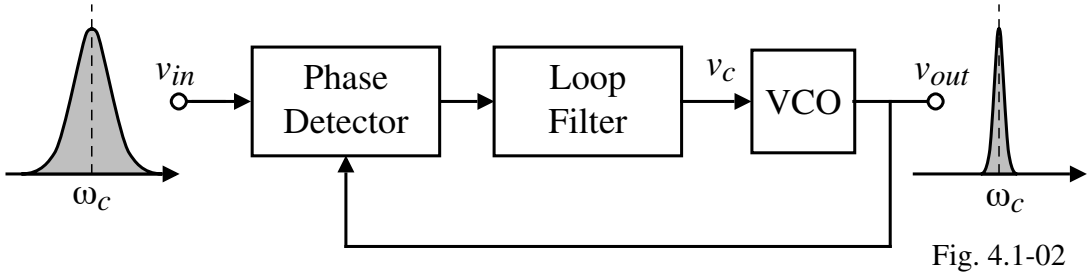


Fig. 4.1-02

This application represents a tradeoff in the capture range and the loop bandwidth.

- If the loop bandwidth is small, the SNR of the output can be much greater than the input.
- If the loop bandwidth is large, the capture range for the desired signal is larger (can track the desired signal better).

Frequency Synthesis

Dividers placed in the feedback and/or input allow the generation of frequencies based on a stable reference frequency.

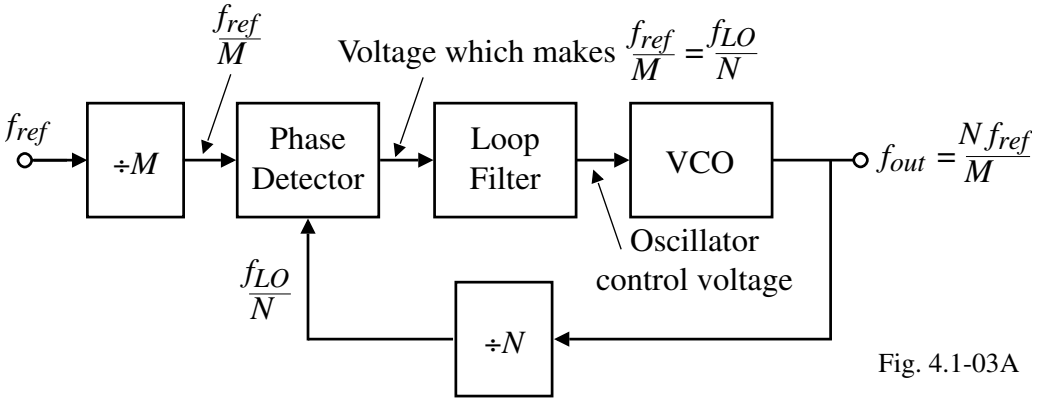


Fig. 4.1-03A

When the phase detector is locked, the two incoming frequencies are equal. Therefore,

$$\frac{f_{ref}}{M} = \frac{f_{out}}{N} \qquad \Rightarrow \qquad f_{out} = \frac{N}{M} f_{ref}$$

Clock and Data Recovery

The function of a clock and data recovery circuit is to produce a stable timing signal from a stream of binary data. Clock recovery consists of two basic functions:

1.) Edge detection

2.) Generation of a stable periodic output

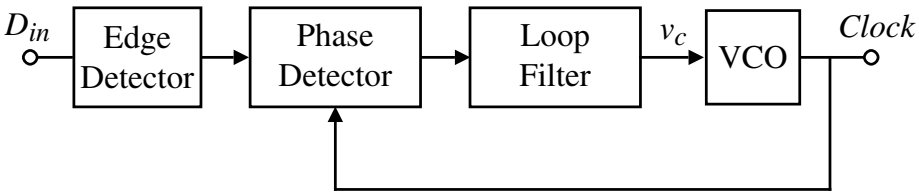


Fig. 4.1-04

Jitter Suppression

In digital communications, transmitter or retrieved data may suffer from timing jitter. A PLL clock recovery circuit can be used to regenerate the signal and eliminate the jitter as shown below.

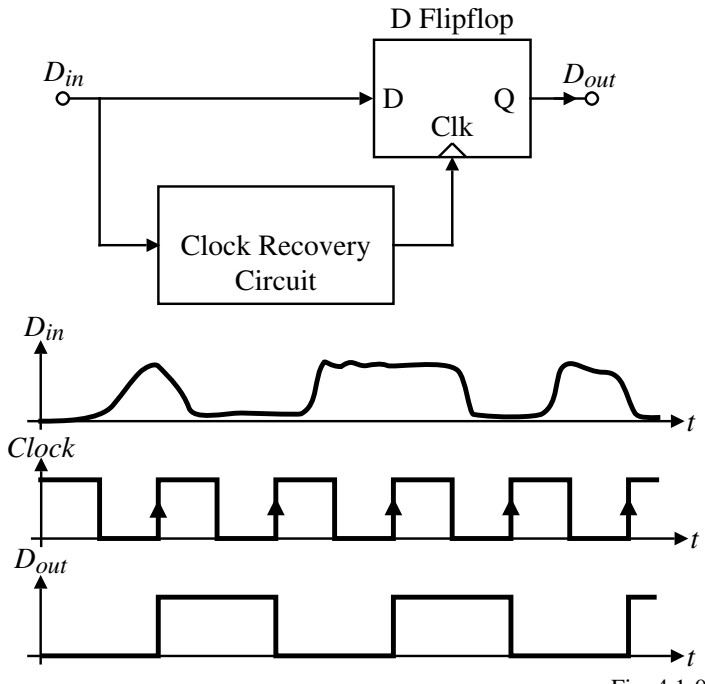


Fig. 4.1-05

Frequency Translation

The PLL can be used to translate the frequency of a highly stable but fixed frequency oscillator by a small amount in frequency. Sometimes called *frequency offset loop*.

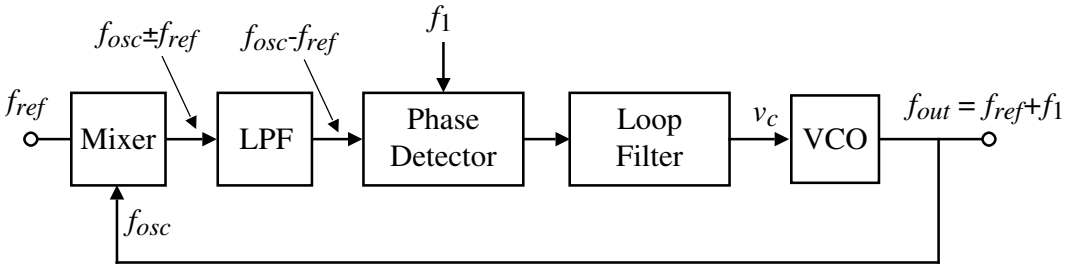


Fig. 4.1-06

IC FREQUENCY SYNTHESIZERS - ARCHITECTURES AND TECHNIQUES

Synthesizer Specifications for Various Wireless Standards

Wireless Standard	Frequency Range (MHz)	Channel Spacing	Number of Channels	Switching Time
GSM	Rx: 935-960 Tx: 890-915	200kHz	124	800µs
DCS1800	Rx: 1805-1880 Tx: 1710-1785	200kHz	374	800µs
PCS1900	Rx: 1930-1990 Tx: 1710-1785	200kHz	-	800µs
DECT	1880-1900	1.728MHz	10	450µs
AMPS	Rx: 869-894 Tx: 824-849	30kHz	832	Slow
CDMA	Rx: 869-894 Tx: 824-849	1.25MHz	20	-
PHS1900	Rx: 1895-1918	300kHz	300	1.5ms
IS54	Rx: 869-894 Tx: 824-849	30kHz	832	Slow
WLAN	2400-2483	1MHz	79	Several µs

Components of a Frequency Synthesizer

Function of a frequency synthesizer is to generate a frequency f_o from a reference frequency f_{ref}.

Block diagram:

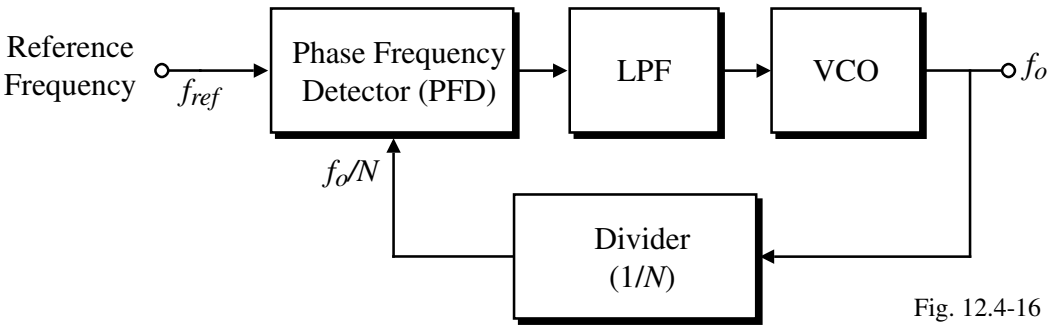


Fig. 12.4-16

Components:

Phase/frequency detector outputs a signal that is proportional to the difference between the frequency/phase of two input periodic signals.

The low-pass filter is use to reduce the phase noise and enhance the spectral purity of the output.

The voltage-controlled oscillator takes the filtered output of the PFD and generates an output frequency which is controlled by the applied voltage.

The divider scales the output frequency by a factor of N.

$$f_{ref} = \frac{f_o}{N} \rightarrow \qquad f_o = N f_{ref}$$

Basic Frequency Synthesizer Architecture

Simple frequency synthesizer:

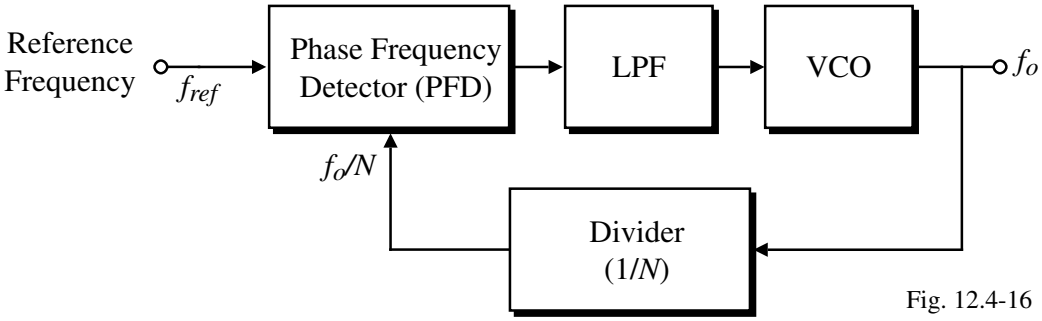


Fig. 12.4-16

Comments:

- Frequency step size is equal to f_{ref}. Thus, for small channel spacing, f_{ref}, is small which makes N large.
- Large N results in an increase in the in-band phase noise of the VCO signal by $20log(N)$.
- $f_o = N \cdot f_{ref}$

Basic Frequency Synthesizer Architecture - Continued

Frequency Synthesizer with a Single-Modulus Prescaler:

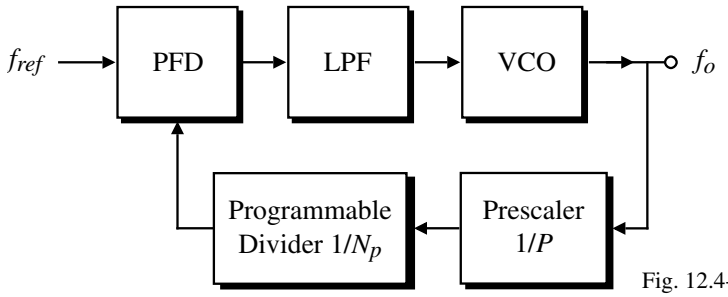


Fig. 12.4-17

Comments:

- $f_o = N_P \cdot P \cdot f_{ref}$
- Only the prescaler needs to run at very high speed
- Since P is fixed, the value of N_P is smaller causing increased channel spacing - results in increased lock-on time and sidebands at undesirable frequencies

Solution:

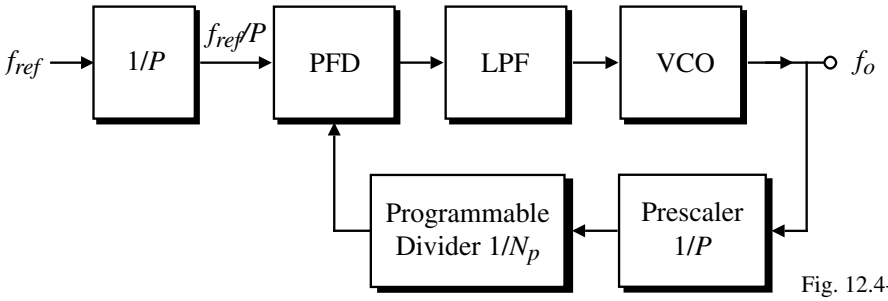


Fig. 12.4-18

Basic Frequency Synthesizer Architecture - Continued

Frequency Synthesizer with a Dual-Modulus Prescaler:

Operation:

1.) The modulus control signal is low at the beginning of a count cycle enabling the prescaler to divide by P +1 until the A counter counts to zero.

2.) The modulus control signal goes high enabling the prescaler to divide by P, until the N_P counter counts down the rest of the way to zero (N_P - A).

3.) Thus, $N = (N_P - A)P + A(P+1) = N_P + A$

$\therefore \quad f_o = (N_P + A) f_{ref}$.

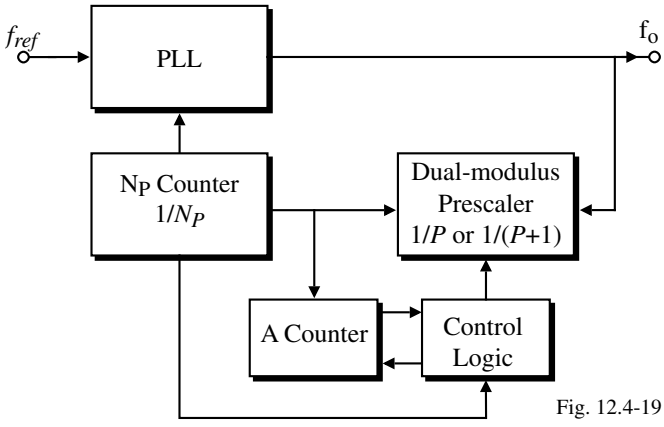


Fig. 12.4-19

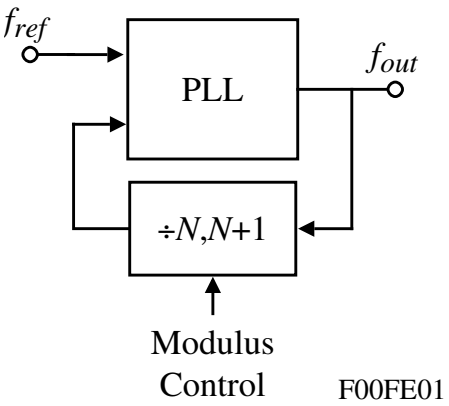
4.) The modulus control is set back low, the counters are reset to their respective programmed values and the sequence is repeated.

Comments:

- $N_P > A$
- The value of P divided by the maximum frequency of the VCO must not exceed the frequency capability of the N_P and A counters.
- P times the period of the maximum VCO frequency > the sum of the propagation delay through the dual-modulus prescaler plus the prescaler setup or release time relative to its control signal plus the propagation delay of f_{ref} to the modulus control.

Example – Dual Modulus Frequency Synthesizer

A block diagram for a dual modulus frequency synthesizer is shown. (a.) If this synthesizer divides the VCO output by N+1 every K VCO cycles and by N for the rest of the time, express the output frequency, f_{out}, as a function of N, K, and f_{ref}. (b.) If you wanted to use this frequency synthesizer to generate an output frequency of 27.135MHz from a reference frequency of 100kHz, what would be the value of N and how many cycles out of 100 would you divide by N+1 where the remaining cycles you would divide by N?



F00FE01

Solution

(a.) The average divide factor is expressed as

N_{eff} = (N+1)xDuty cycle for N+1 + NxDuty cycle for N

$$= (N+1)\left(\frac{1}{K}\right) + N\left(1 - \frac{1}{K}\right) = N + \frac{1}{K} \qquad \therefore \boxed{f_{out} = N_{eff} f_{ref} = \left(N + \frac{1}{K}\right) f_{ref}}$$

(b.) Dividing 27.135MHz by 100kHz gives 271.35. Therefore, choose N = 271 and divide by N+1 or 272 for 35 cycles out of 100 and by N for the remaining 65 cycles. Thus,

$\boxed{N = 271 \text{ and } K = 35 \text{ cycles for every } 100 \text{ cycles}}$

Fractional-N Frequency Synthesizer

The output frequency can be finer than f_{ref} because division ratio in the feedback loop does not have to be an integer.

Operation:

Make the division ratio alternate between N or N +1 in a controlled and repetitive fashion to average an intermediate value between N and N +1.
For example, assume that the synthesizer divides by N +1 every L cycles and by N the rest of the time. The average division ration is $N_{aver} = N + \frac{1}{L}$.

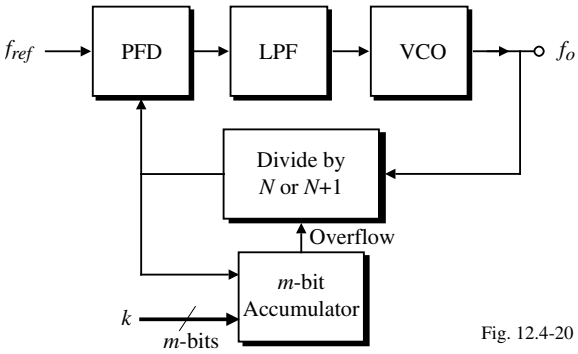


Fig. 12.4-20

Therefore,

$$f_o = \left[(N+1)\left(\frac{1}{L}\right) + N\left(1 - \frac{1}{L}\right)\right] f_{ref} = \left(N + \frac{1}{L}\right) f_{ref}$$

Fractional-N Techniques:

Technique	Feature	Problem
DAC phase estimation	Cancel spurs by DAC	Analog mismatch
Random Jittering	Randomize divider	Frequency jitter
$\Delta\Sigma$ modulation	Modulate the divider ratio	Quantization noise
Phase interpolation	Inherent fractional divider	Interpolation jitter
Pulse generation	Insert pulses	Interpolation jitter

A 1 GHz Fractional-N Frequency Synthesizer

Block diagram:

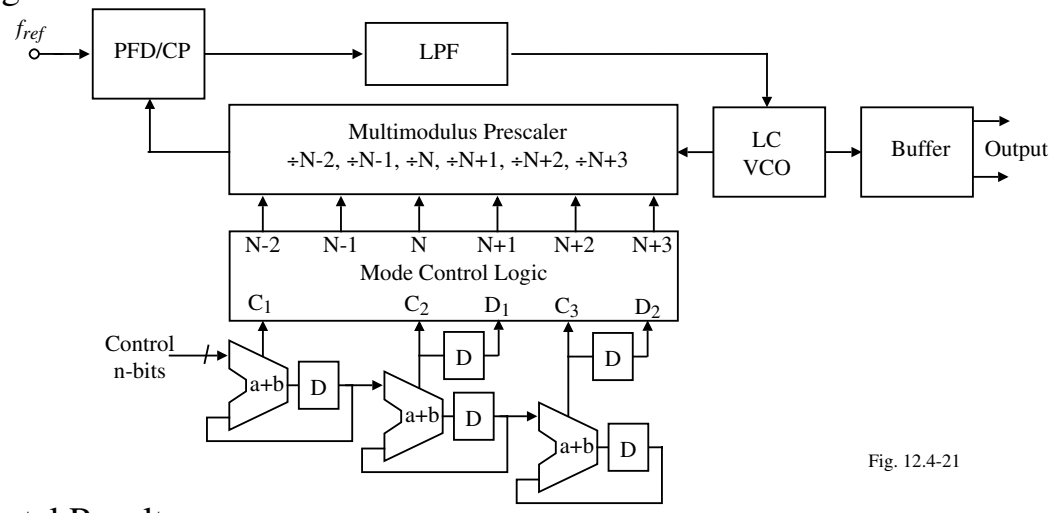


Fig. 12.4-21

Experimental Results:

Carrier Frequency	Phase Noise, 10kHz offset	Phase Noise, 100kHz offset	Phase Noise, 200kHz offset	Phase Noise, 600kHz offset	Phase Noise, 1MHz offset
972 MHz	-83.1dBc/Hz	-104.1dBc/Hz	-110dBc/Hz	-188dBc/Hz	-122.4dBc/Hz
916MHz	-84.6dBc/Hz	-104.4dBc/Hz	-110.4dBc/Hz	-118.2dBc/Hz	-122.7dBc/Hz

Sideband spurs < -70dBc, power supply range of 2.7 to 4.5V (5.2mA at 3V), tuning range 0.88-1GHz

A Low-Noise, 1.6 GHz CMOS Frequency Synthesizer†

A CMOS PLL used to design the front-end RF function of frequency synthesizer.

Block Diagram:

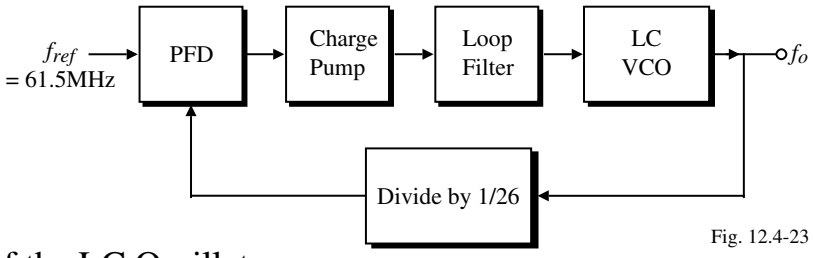


Fig. 12.4-23

Circuit Diagram of the LC Oscillator:

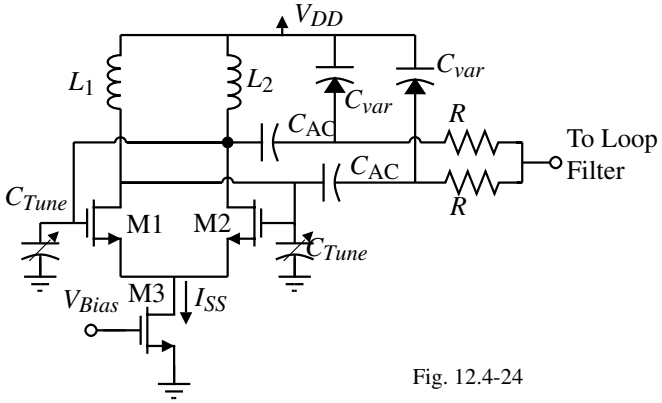


Fig. 12.4-24

Performance:

- Power supply - 2.7V to 5V
- Power dissipation at 3V is 90mW
- Phase noise of -105dBc/Hz at 200kHz offset
- Tuning range of 1.6GHz±100MHz
- 1.5mm^2 in 0.6μm CMOS technology

† J.Parker and D.Ray, "A Low-Noise 1.6 GHz CMOS PLL with On-Chip Loop Filter, *Proc. of 1997 Conf. on Custom Integrated Circuits*, May 1997.

Comparison of Recent CMOS VCO Noise Results

Author	Power Dissipation P	Freq-uency f_0	Phase Noise to Carrier Ratio	Offset Freq. (f)	Estimated Open Loop Q	K_0
Craninckx, Steyart, ISSCC95	24mW @3V	1.8 GHz	-85dBc	10kHz	10	4×10^{-15}
Rael, Abidi, ISSCC96	43mW@3V	900MHz	-100dBc/Hz	100kHz	4	1.7×10^{-15}
Souyer, ISSCC96	24mW@3V	4GHz	-106dBc/Hz	1MHz	7	1.2×10^{-15}
Thamsirianut, CICC94	7.5mW@3V	900MHz	-93dBc/Hz	100kHz	1 (Class B ring osc.)	0.3×10^{-15}
Weigandt, ISCAS94	10mW@3V	1GHz	-85dBc/Hz	100kHz	1 (Class A ring osc.)	2.5×10^{-15}
Parker, Ray, CICC97	90mW@3V	1.6GHz	-105dBc/Hz	200kHz	≈7	0.6×10^{-15}
Park, CICC98	17mW@3V	980MHz	-109dBc/Hz	200kHz	8	0.2×10^{-15}

$$\frac{\text{Phase Noise}}{\text{Carrier Amplitude}} = K_0 \left(\frac{f_0}{f}\right)^2 \frac{1}{PQ}$$

DIVIDERS FOR FREQUENCY SYNTHESIZERS

Introduction

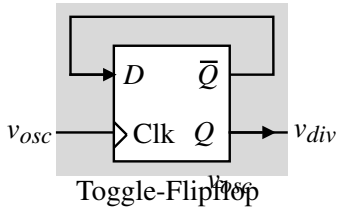
We have seen that in the previous material that dividers can be either fixed or programmable.

In this section we will focus on circuits and concepts suitable for fixed, integer and fractional-N dividers.

In addition, we shall consider noise-shaping techniques using delta-sigma methods applied to the fractional-N technique.

Fixed Dividers

Toggle-Flipflop based divide-by-2:



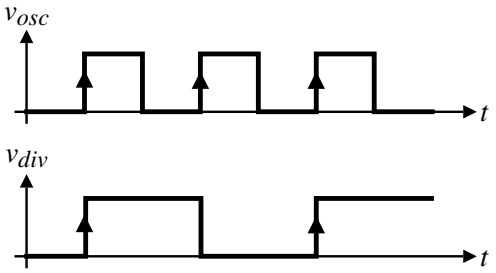


Fig. 4.3-11

D-Flipflop Implementation:

- Proper sizing of the transistors results in reasonable power-speed tradeoffs at GHz rates.
- Device mismatches can result in phase imbalances as large as 5°.
- If the Clk input is not perfectly differential, additional phase unbalances can occur.

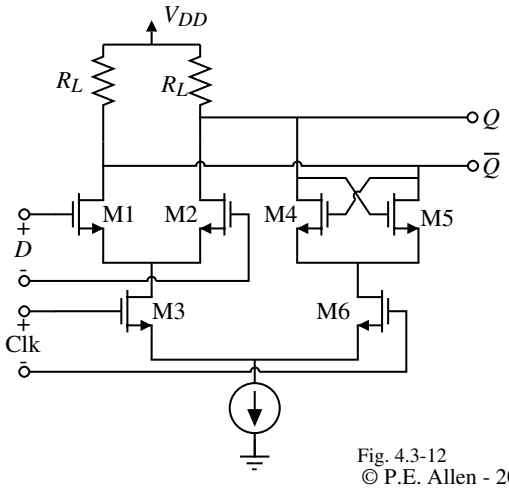


Fig. 4.3-12

Dual Modulus Dividers

Evolution of a divide-by-2/3 from a divide-by-3 circuit:

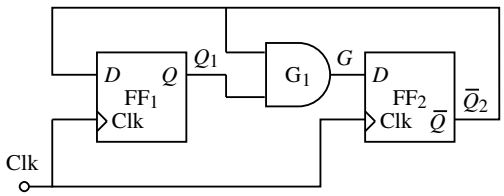
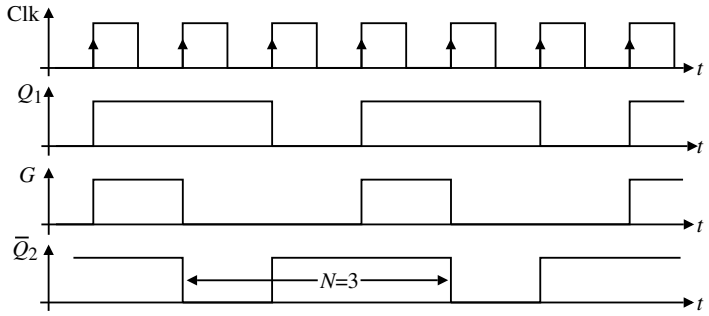


Fig. 4.3-13



Divide-by-2/3 circuit (MC=1 → ÷2, MC=0 → ÷3):

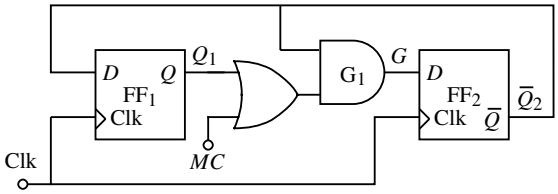
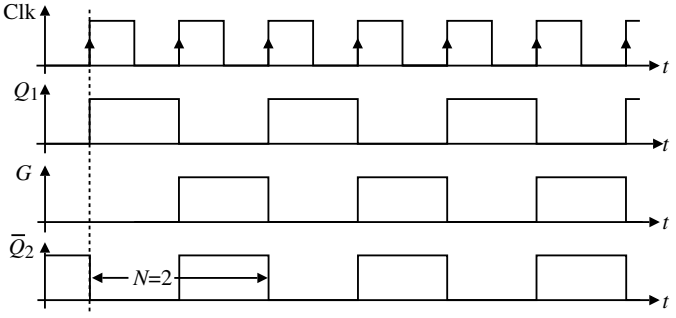


Fig. 4.3-14



Dual Modulus Dividers - Continued

State diagram of the divide by 2/3 circuit:

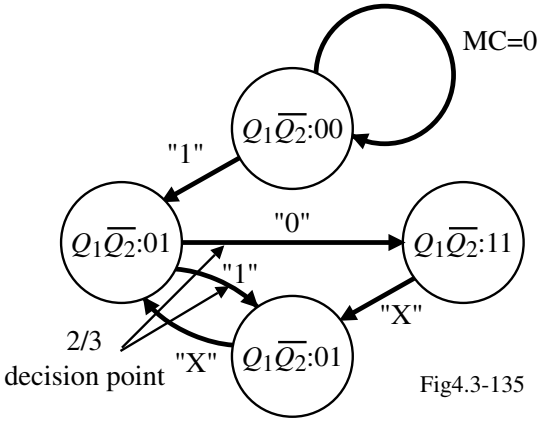


Fig4.3-135

Speed of the Dual Modulus Divider

The divide-by-3 circuits are generally much slower than their divide-by-two counterparts. Consider the implementation of part of the previous divide-by-2/3 circuit.

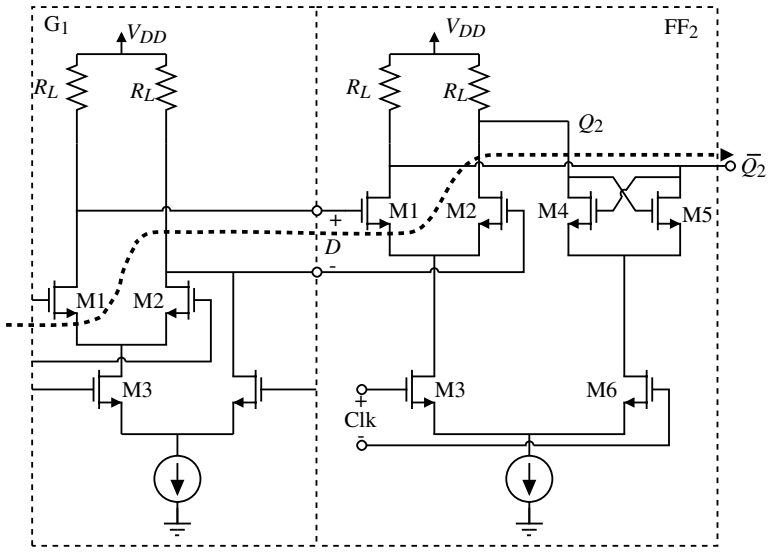


Fig. 4.3-15

On the clock edge where $\overline{Q_2}$ must change, sufficient time must be allowed for the delay of the AND gate, G_1, and the input stage of FF2 before the next clock transition.

It is seen that the delay for ÷3 circuit is nearly twice that of the ÷2 circuit.

Programmable Dividers

A divider can be achieved by using a programmable counter.

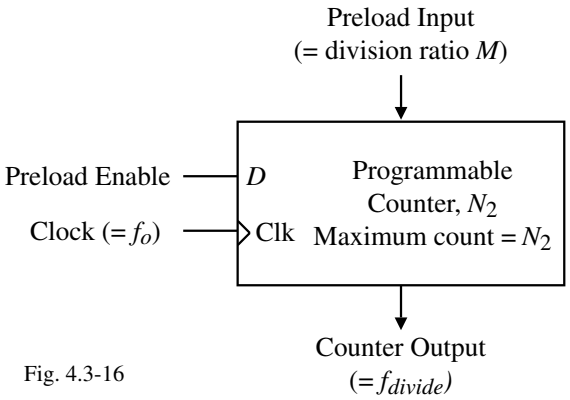


Fig. 4.3-16

For a given speed requirement, a programmable divider is less power optimized because the critical path is dependent on the loaded value.

A complete divider consisting of a fixed divider cascaded with a programmable divider.

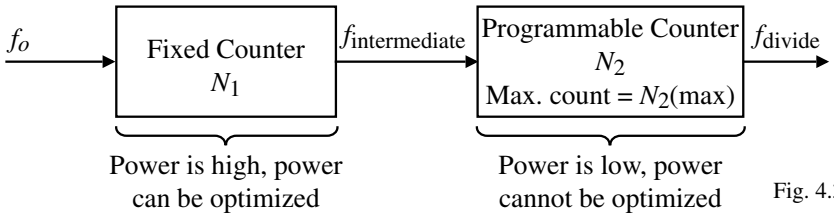


Fig. 4.3-17

Resolution (Complete divider)

= Resolution (programmable divider) x Division ratio (fixed divider)

Waveforms of Various Complete Dividers

$N_1 = 3$ and $N_2 = 4$:

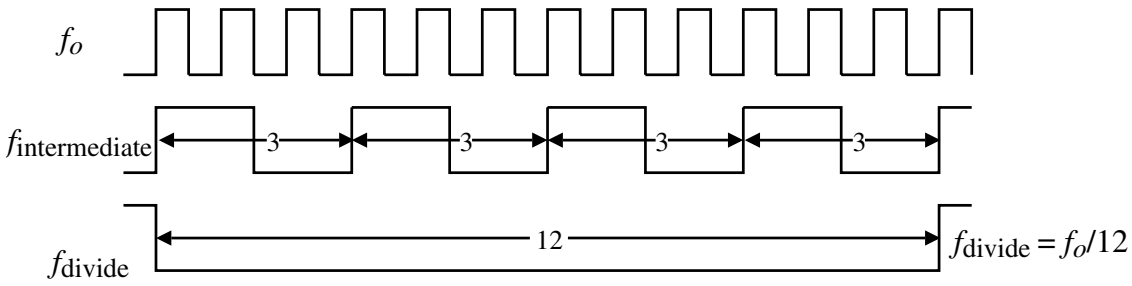


Fig. 4.3-18

$N_1 = 3$ and $N_2 = 3$:

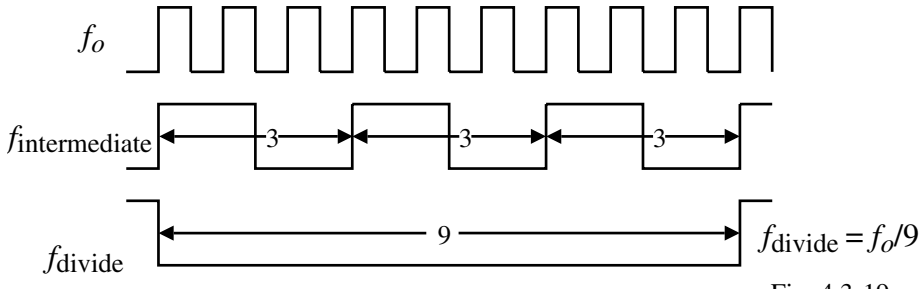


Fig. 4.3-19

Waveforms of Various Complete Dividers – Continued

$N_1 = 3/4$ ($N_1 = 4$ for one N_2 cycle) and $N_2 = 3$:

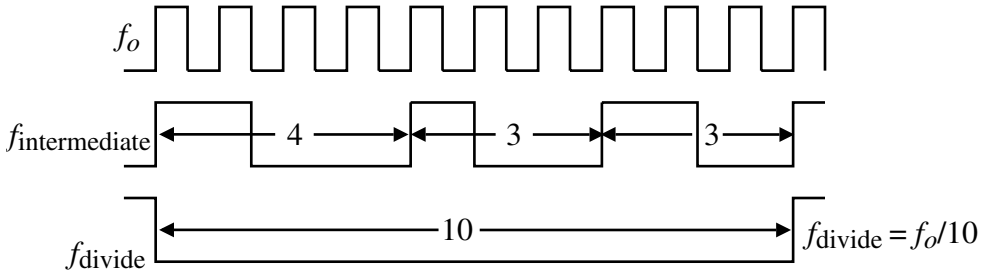


Fig. 4.3-20

$N_1 = 3/4$ ($N_1 = 4$ for two N_2 cycles) and $N_2 = 3$:

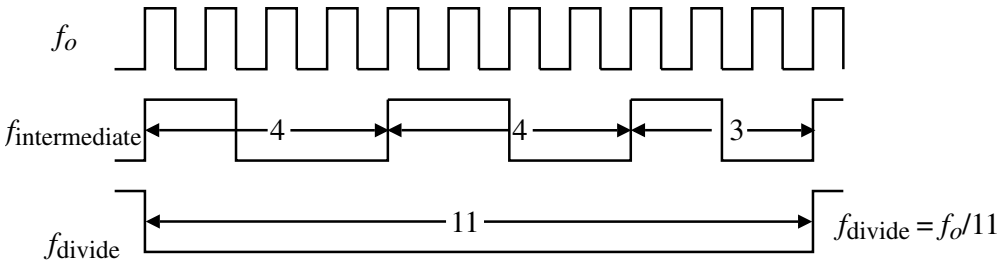


Fig. 4.3-20

Multi-Modulus Dividers

÷4/÷5 dual modulus counter example:

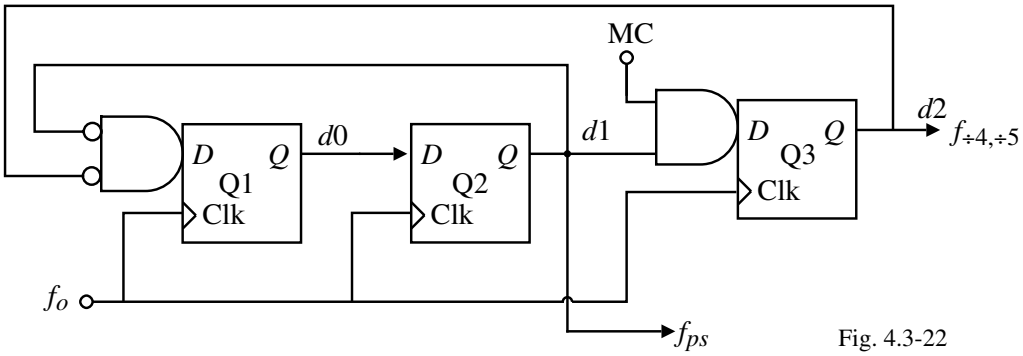


Fig. 4.3-22

State Diagram:

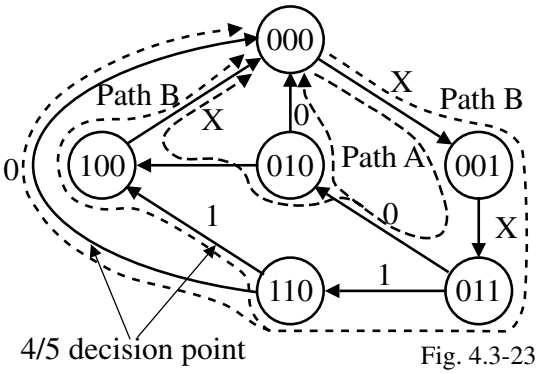


Fig. 4.3-23

Note that there are two possible state paths A and B each consisting of two sequences, a ÷4 sequence and a ÷5 sequence.

For path A, the ÷4 sequence is from 000, 001,011, 010, 000 and the ÷5 sequence is from 000, 001, 011, 010, 100, 000.

For path B, the ÷4 sequence is from 000, 001, 011, 110, 000 and the ÷5 sequence is from 000, 001, 011, 110, 100, 000.

NOISE SHAPING TECHNIQUES

Delta-Sigma Shaping Techniques

Delta-sigma modulators can be used along with mulitmodulus dividers to achieve noise shaping of phase noise.

The objective of the delta-sigma modulator is to remove the noise due to the fluctuation of the mulitmodulus dividers.

The following slides review this technique as applied to frequency synthesizers.

Analog implementation of a first-order delta-sigma modulator:

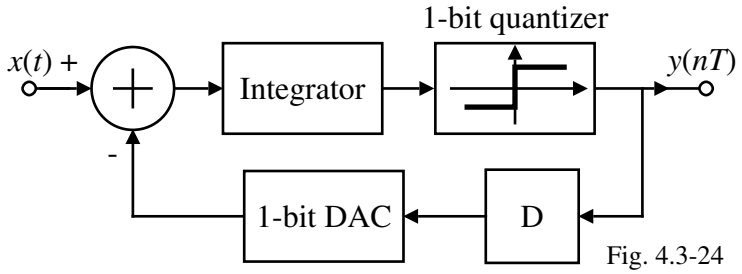


Fig. 4.3-24

Digital Implementation of the Delta-Sigma Modulator

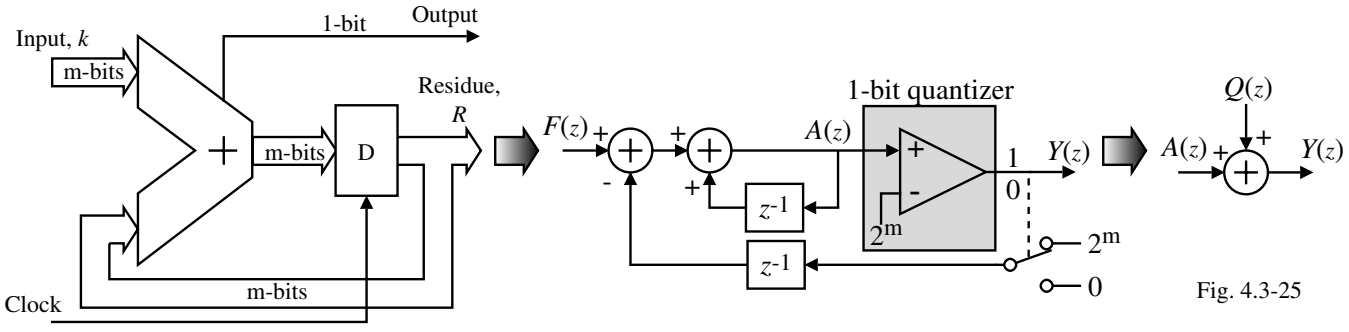


Fig. 4.3-25

The discrete first-order delta-sigma modulator can be implemented with an *m*-bit accumulator. The *m*-bit accumulator has m input bits, a single output bit (carry-bit or MSB), and *m*-residue bits.

Operation:

On every cycle of the reference clock, the residue output *R* of the accumulator is assigned the value *R*+*k* after one cycle if an overflow does not occur or the value $R+k-2^m$ if the accumulator produces a carry-bit signal.

Therefore, the accumulator overflow is equivalent to the comparator decision. The data stored in the accumulator is essentially the integral of the error between the desired frequency data *k* and the actual frequency control input.

High-Order Delta-Sigma Modulators

z-transform of a first-order delta-sigma modulator:

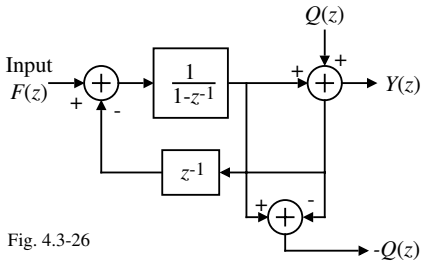


Fig. 4.3-26

n-th order delta-sigma modulator:

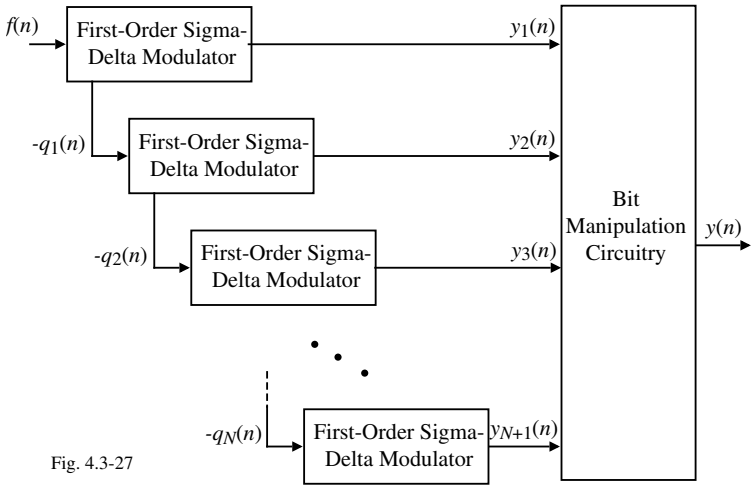


Fig. 4.3-27

Use of a Modulator for Divider Control

Consider the second-order delta-sigma modulator implemented with m-bit accumulators:

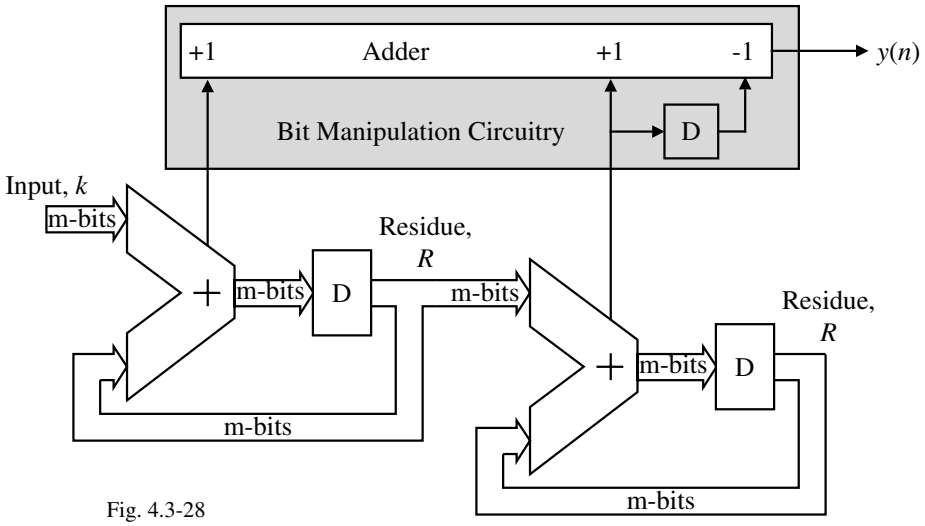


Fig. 4.3-28

Use of a Modulator for Divider Control – Continued

z-tranform model for the previous second-order delta-sigma modulator:

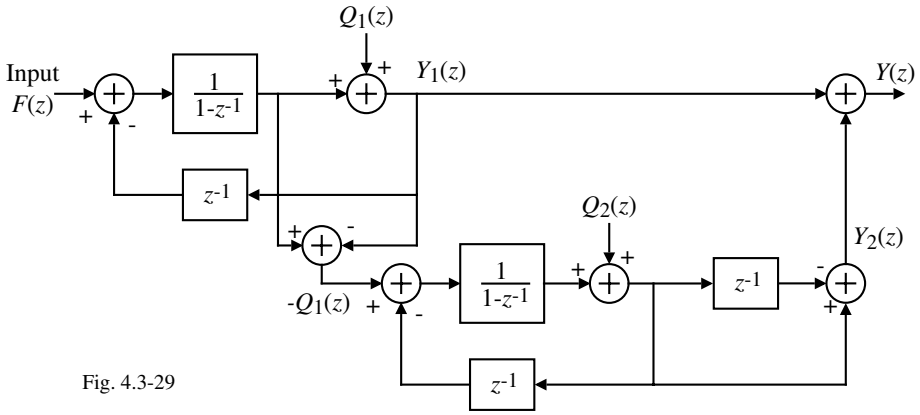


Fig. 4.3-29

From the above diagram, we can write,

$$Y_1(z) = F(z) + (1-z^{-1})Q_1(z) \qquad \text{and} \qquad Y_2(z) = -Q_1(z)(1-z^{-1}) + Q_2(z)(1-z^{-1})^2$$

can be combined to give,

$$Y(z) = F(z) + + Q_2(z)(1-z^{-1})^2$$

Generalizing to the n-th order gives,

$$Y(z) = F(z) + + Q_n(z)(1-z^{-1})^n$$

Use of a Modulator for Divider Control – Continued

The effective divide ratio of a fractional divider implemented with an n-th order delta-sigma modulator can be written as,

$$N_{eff} = N(z) + Y(z) = N(z) + F(z) + Q_n(z)(1-z^{-1})^n$$

where

$N(z)$ = integer part of the divide ratio

$F(z)$ = fractional part of the divide ratio

$Q(z)$ = quantization noise occurring at the n-th delta-sigma modulator

If the PLL is in lock, then

$$f_o = N_{eff} \cdot f_{ref} = [N(z) + F(z)]\, f_{ref} + (1-z^{-1})^n Q_n(z)\, f_{ref}$$

where the first term is the desired frequency and the second term represent the frequency fluctuation resulting from the quantization noise in the fractional modulator.

Use of a Modulator for Divider Control – Continued

Assume that the quantization noise is a random quantity in the interval $\{-0.5\Delta, +0.5\Delta\}$ with equal probability. If the quantizer is 1-bit, then Δ which is the quantization step size is 1.

The noise power or variance, σ_e^2, can be found as

$$\sigma_e^2 = E(e) = \frac{1}{\Delta}\int_{-0.5\Delta}^{0.5\Delta} e^2 de = \frac{\Delta^2}{12}$$

The spectrum of the quantization noise is where $N(f)$ is given as,

$$N(f) = \frac{\Delta^2}{12 f_{ref}}$$

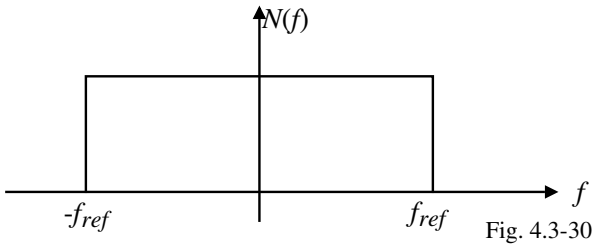


Fig. 4.3-30

where f_{ref} is the sampling frequency which is equal to the comparison frequency of the PFD.

Use of a Modulator for Divider Control – Continued

Define $\Delta f(z)$ as the frequency noise of fluctuation of the output frequency $f_o(z)$. The power spectral density, $S_{\Delta f(z)}$, can be calculated from the second term of the previous expression for $f_o(z)$.

$$\therefore \quad S_{\Delta f(z)} = |(1-z^{-1})^n f_{ref}|^2 \frac{\Delta^2}{12 f_{ref}} = |(1-z^{-1})^n f_{ref}|^2 \frac{1}{12 f_{ref}} = |(1-z^{-1})|^{2n} \frac{f_{ref}}{12}$$

Because phase is related to frequency through integration, the phase noise, $\theta_n(t)$, is

$$\theta_n(t) = 2\pi\int \Delta f(t) dt$$

Using a simple rectangular integration in the z-domain yields,

$$\Theta_n(z) = \frac{2\pi\,\Delta f(z)}{f_{ref}(1-z^{-1})}$$

The power spectral density of the phase noise, $S_{\Theta_n(z)}$, can be written as,

$$S_{\Theta_n(z)} = |\Theta_n(z)|^2 S_{\Delta f(z)} = \frac{(2\pi)^2}{f_{ref}^2 |1-z^{-1}|^2} S_{\Delta f(z)} = \frac{(2\pi)^2 |1-z^{-1}|^{2(n-1)}}{12 f_{ref}} \text{ rads}^2/\text{Hz}$$

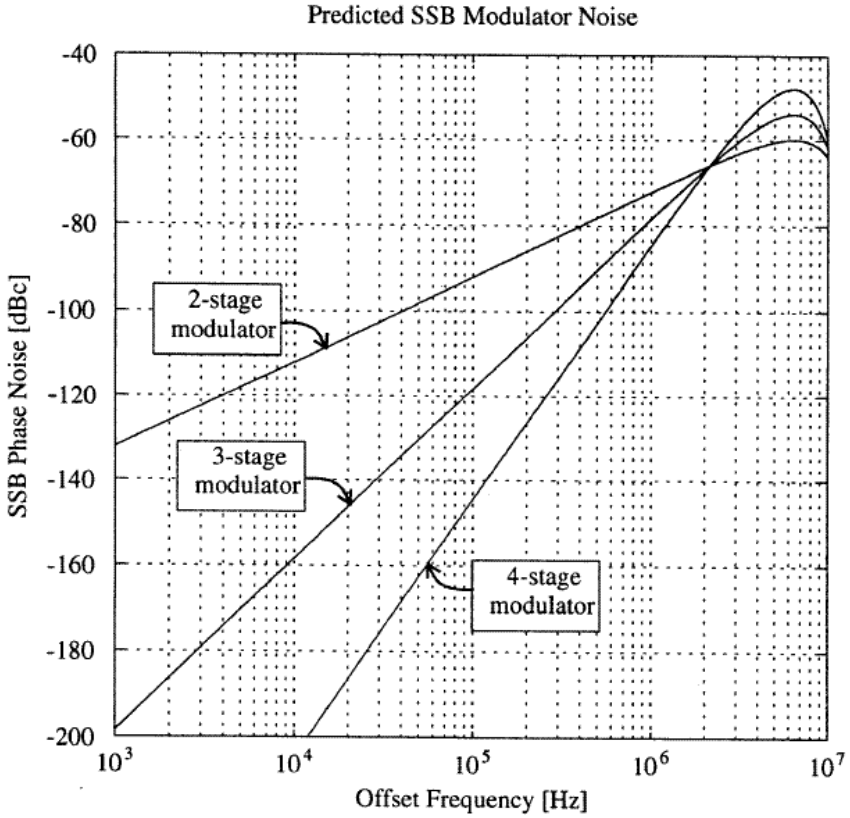
Assuming $S_{\Theta_n(f)}$ is a two-sided power spectral density function gives $\mathcal{L}(f) = S_{\Theta_n(f)}$

$$\therefore \qquad \mathcal{L}(f) = \frac{(2\pi)^2}{12 f_{ref}}\left[2\sin\left(\frac{\pi f}{f_{ref}}\right)\right]^{2(n-1)} \text{ rads}^2/\text{Hz}$$

where z^{-1} has been replaced with $e^{-j2\pi f/f_{ref}}$ and n is the order of the modulator.

Use of a Modulator for Divider Control – Continued

Predicted phase noise of higher-order modulators (f_{sample} = 12.8 MHz):



Use of a Modulator for Divider Control – Continued

Results:

If a modulator has an accumulator input data k consisting of m bits, then the oscillator output frequency, f_o, can be given as,

$$f_o = \left(N + \frac{k}{2^m}\right) f_{ref}$$

The uncertainty of this frequency will be reduced by the use of the sigma-delta modulator.

Summary:

- The delta-sigma modulator attenuates phase noise from the factional controller to negligible levels close to the center frequency.
- Further from the center frequency, the phase noise increase rapidly and must be filtered out prior to tuning the input of the VCO.
- The loop filter in the PLL is used to filter the noise away from the center frequency.
- When a higher-order, delta-sigma modulator is used for a fractional-N controller, the PLL needs more poles in the loop filter to suppress the quantization noise at high frequencies.

SUMMARY

- Examine the applications of PLLs
  1.) Demodulation and modulation
  2.) Signal conditioning
  3.) Frequency synthesis
  4.) Clock and data recovery
  5.) Frequency translation
- Integrated Circuit Frequency Synthesizers – Architectures and Techniques
  - Fractional N
  - Dividers/prescalers
  - Noise shaping techniques