High Frequency Voltage Controlled Ring Oscillators in Standard CMOS

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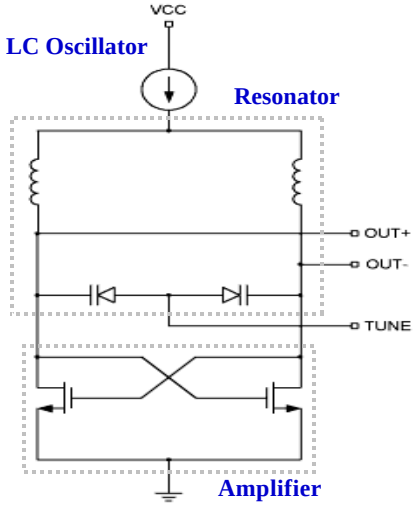
Agenda

- Integrated VCO types
- Ring oscillator theory
- Important characteristics of ring oscillators
  - Frequency
  - Noise
- High frequency low noise ring oscillators
- Prototype Chip
- Performance Comparison
- Applications/Summary/Conclusions

Integrated VCO Types

- LC Oscillator
- Ring Oscillator

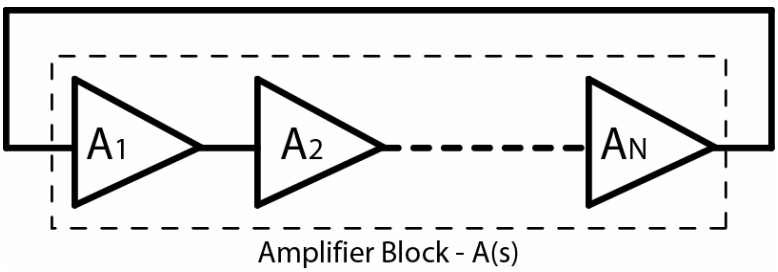
VCO Types : LC



- High Q resonant element
- Expensive to implement
  - Require more die area
  - Reduce integration density
  - Extra steps
- Secondary effects
  - Eddy currents
  - Magnetic coupling

VCO Types : Ring

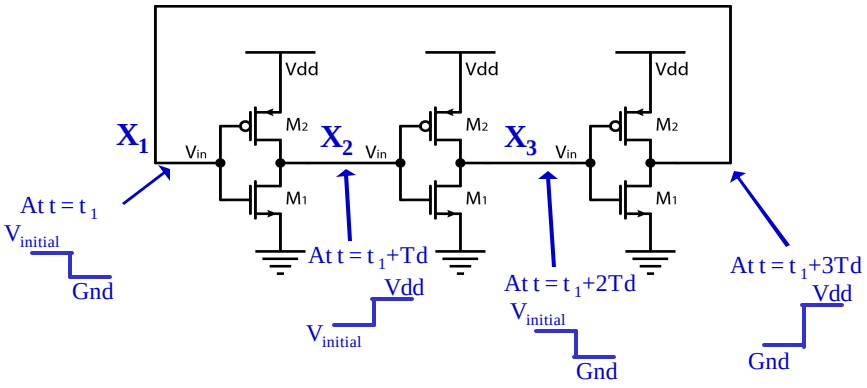
Ring Oscillator



- Less expensive to implement
- Wider tuning range
- Multiple output phases
- Low Q

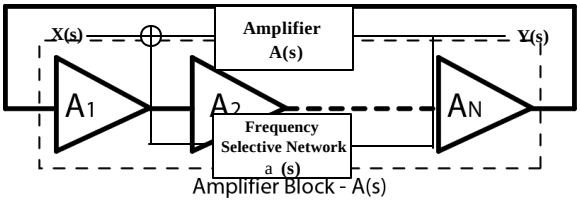
Ring Oscillator Theory

Ring Oscillator Operation in Time Domain



- **Odd number of inversions**
- **T = 6*Td or 2N*Td for N stage**
- **f_{osc} = 1/(6*Td) or 1/(2N*Td) for N stage**

S-domain Analysis : Ring Oscillator



$$L(s) = A_1(s)A_2(s)...A_N(s)$$

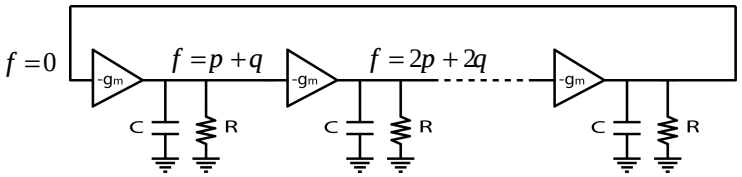
$$= A^N(s) \text{ assuming that } A_1(s) = A_2(s) = ... = A_N(s)$$

Barkhausen Criterion:

$$\angle A(jw_0) = q = \frac{2kp}{N} \text{ and } |A(jw_0)|^N = 1$$

at the oscillation frequency

Ring Oscillator Linear Model



$f = N(p+q)$

$= N(p + \frac{p}{N})$

$= 0$

for odd # of stages

Stage transfer function $A(jw) = \left[\frac{-g_m R}{1 + RCjw}\right]$

$q = \frac{p}{N}$

Frequency : $w_0 = \frac{\tan q}{RC}$

Gain requirement : $g_m R \geq \frac{1}{\cos q}$

For 3-stage $w_0 = \sqrt{3}/RC$

For 3-stage $g_m R \geq 2$

For 4-stage $w_0 = 1/RC$

For 4-stage $g_m R \geq \sqrt{2}$

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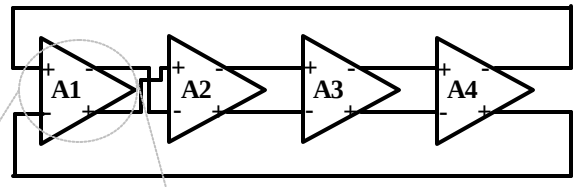
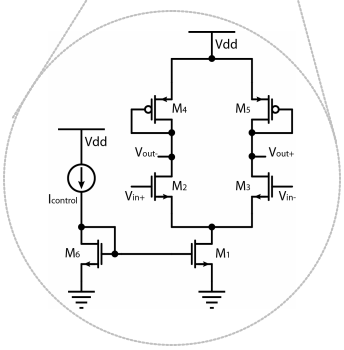
Differential Ring Oscillators





- **Better immunity to common-mode disturbance**
- **50% duty cycle**
- **Improved spectral purity**
- **Even/Odd number of stages**

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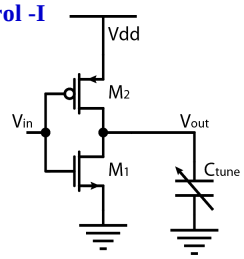
Important Characteristics of Ring VCOs

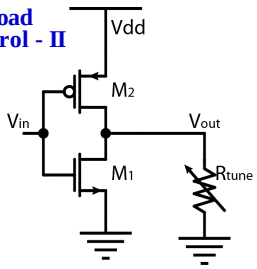
- **Frequency**

Frequency Tuning - I

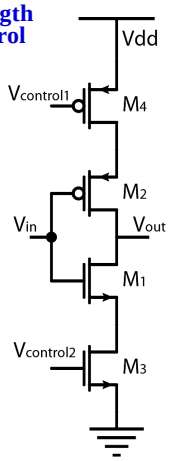
Load Control -I



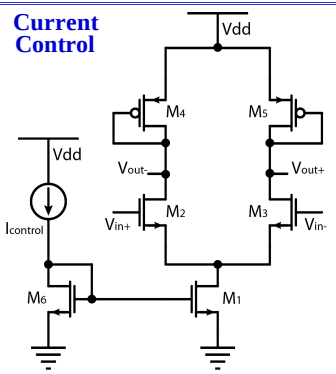
Load Control - II



Drive Strength Control



Current Control

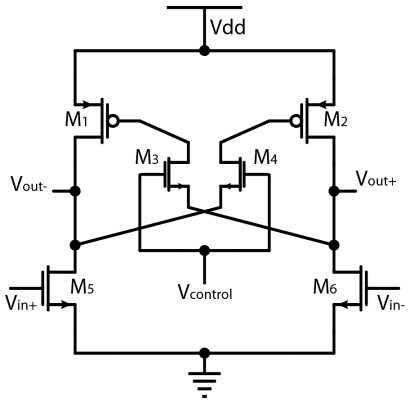


$$T_d = \frac{C_L V_{swing}}{I_{control}}$$

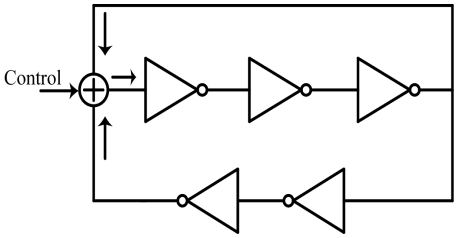
$$f_{osc} = \frac{I_{control}}{2NC_L V_{swing}}$$

Frequency Tuning - II

Feedback Control



Coupling Control



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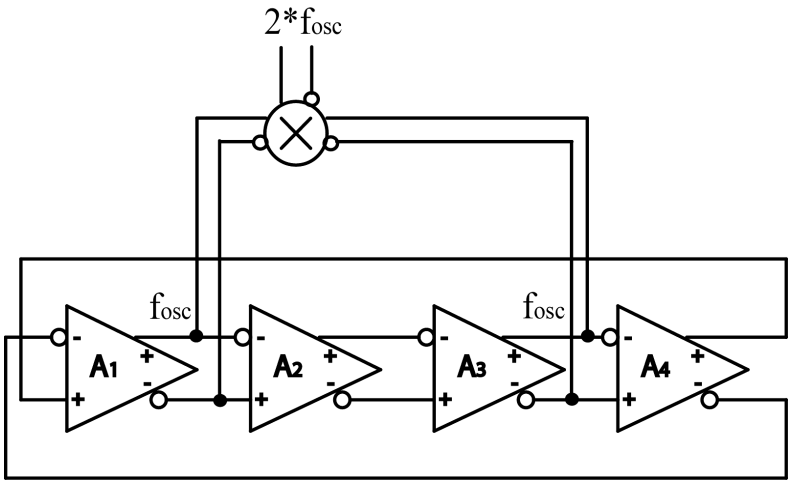
Frequency Increase : Multipliers



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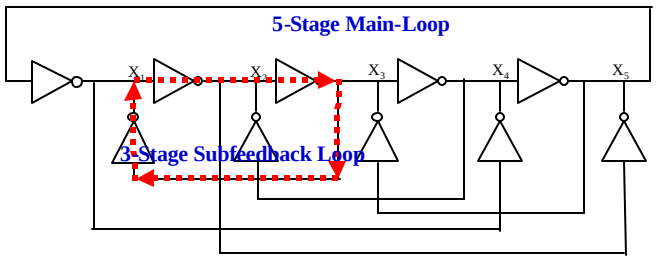
Frequency Increase : Subfeedback Loops[1]

Implementation with N = 5, i = 2



[1] L. Sun, T. Kwasniewski, and K. Iniewski, "A Quadrature Output Voltage Controlled Ring Oscillator Based on Three-Stage Subfeedback Loops," *Proc. Int. Symp. Circuits and Systems*, Orlando, FL, 1999, vol. 2, pp. 176-179.

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Important Characteristics of Ring VCOs

- **Noise**

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Phase Noise : Leeson's Model

Single Sideband Oscillator Phase Noise in Leeson's Model

$$L\{\Delta w\} = \frac{2FkT}{P_S}\left(\frac{w_0}{2Q\Delta w}\right)^2$$

Q of LC Oscillators

$$Q \le 10$$

(standard CMOS)

Q of a ring oscillator?

Ring Oscillator Q : Razavi

Q of a ring oscillator

$$Q = \frac{w_0}{2}\sqrt{\left(\frac{dA}{dw}\right)^2 + \left(\frac{df}{dw}\right)^2}$$

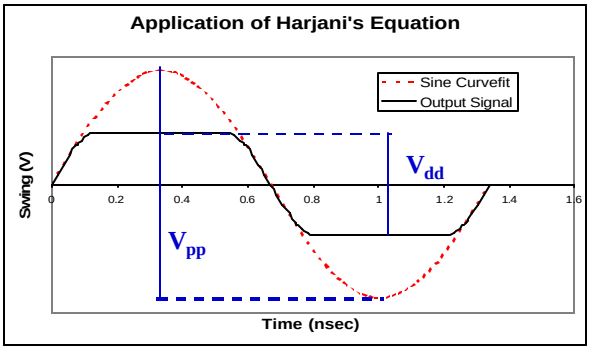
Modified Leeson's equation

$$L\{\Delta w\} = \frac{2NFkT}{P_S}\left(\frac{w_0}{2Q\Delta w}\right)^2$$

3-stage Q : $3\sqrt{3}/4 \cong 1.3$

4-stage Q : $\sqrt{2} \cong 1.4$

Phase Noise : Harjani



$$L\{\Delta w\} = \begin{cases} \frac{64\,FkTR}{9V_{pp}^2}\left(\frac{w_0}{\Delta w}\right)^2 & \left(for\ V_{pp} << \frac{8*V_{dd}}{3p}\right) \\ \frac{512\,FkTRV_{dd}}{27pV_{pp}^3}\left(\frac{w_0}{\Delta w}\right)^2 & \left(for\ V_{pp} >> \frac{8*V_{dd}}{3p}\right) \end{cases}$$

$$V_{pp} = \frac{2SR_{MAX}}{w_0}$$

Equation from : L. Dai, and R. Harjani, "Design of Low-Phase-Noise CMOS Ring-Oscillators," *IEEE Trans. Circuits Sys. II*, vol. 49, pp. 328 -338, May 2002.

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Ring Oscillator Q : Harjani

Q of a 3-stage ring oscillator

$$Q_{eff} = \frac{9}{8}\sqrt{\frac{p\left|dv/dt\right|_{\max}}{w_0 V_{dd}}}$$

$$Q_{eff}(3\text{-stage rings, at } 900\text{ MHz}) = \begin{cases} 3.63 \text{ in TSMC } 0.18\text{um} \\ 3.02 \text{ in TSMC } 0.25\text{um} \\ 2.51 \text{ in TSMC } 0.35\text{um} \end{cases}$$

- **Clipped Signals**
- **Sharper transition**
- **Full-switching**

→ **Better NOISE performance!!**

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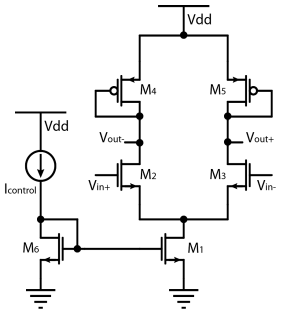
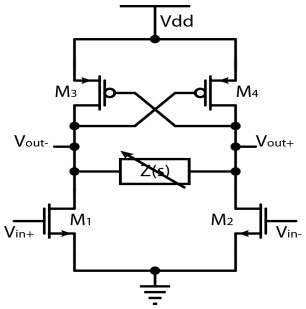
Ring Oscillator Gain Stages

Analog Gain Stage



Saturated Gain Stage



- Stage gain dependence for switching
- Inferior noise performance
  - Continuous conduction
  - Cascaded connections
- Latching characteristics speed-up signal transitions
- Good noise characteristics
  - Full Switching
  - Rail-to-rail outputs

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High Frequency Low Noise Ring Oscillators

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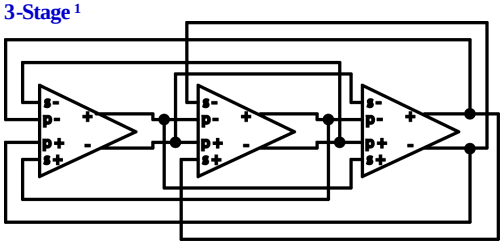
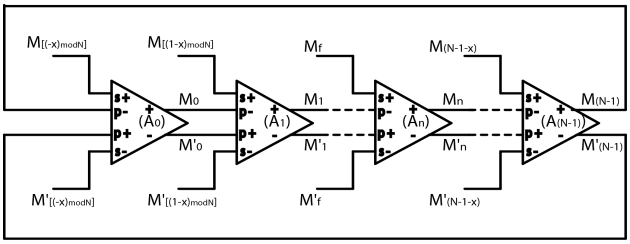
Multiple-Pass Loop Architecture

3-Stage [1]



- **Auxiliary loops nested inside main-loop**
- **Frequency Improvement**
  - **Effective stage delay reduced**
- **Noise Improvement**
  - **Slew Rate increase**

General



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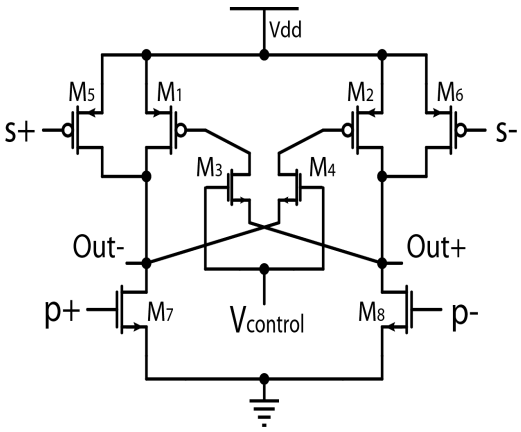
Saturated Gain Stage with Regenerative Elements



- **Used in our designs**
- **Frequency control by varying latch strength**
- **Two sets of inputs for multiple-pass architecture**
- **Tuning range control by varying sizes of M3 and M4.**

Delay Stage : C.H. Park, and B. Kim, "A Low-Noise, 900-MHz VCO in 0.6 μm CMOS," *IEEE J. Solid State Circuits*, vol. 34, pp. 586-591, May 1999.

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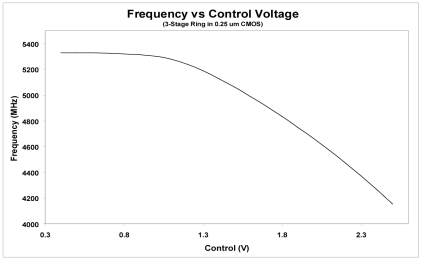
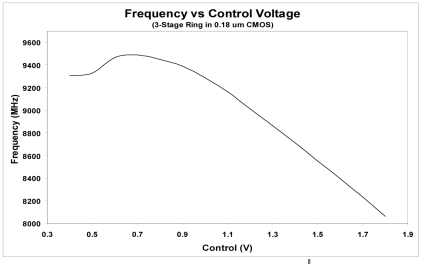
Multiple-Pass Ring Oscillator with Saturated Gain Stage – Frequency/Noise Performance

Number of Stages	Technology, CMOS	Frequency Range (GHz)	Phase Noise at 1 MHz (-dBc/Hz)
3	0.25 um	4.15-5.30	-105.2 (5.07 GHz)
4	0.25 um	2.50-3.68	-110.28 (3.42 GHz)
3	0.18 um	8.10-9.50	-99.2 (9.05GHz)
4	0.18 um	5.56-6.66	-104.66 (6.35 GHz)
4	0.18 um	4.11-6.53	-104.21 (5.29 GHz)
5	0.18 um	-	-113.46 (4.33 GHz)
3	0.13 um	8.75-14.4	-90.49 (10.97 GHz)





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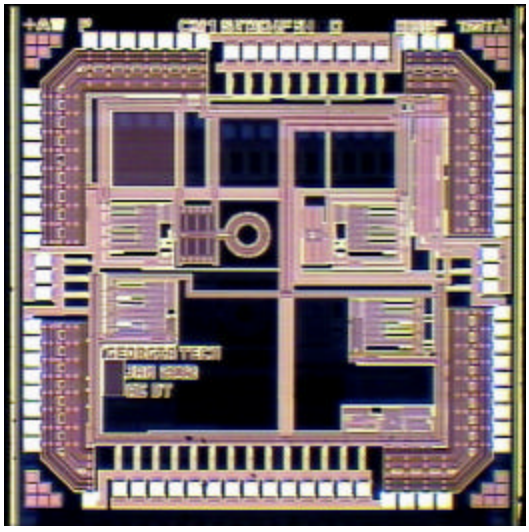
Prototype Chip



- 0.18 µm TSMC CMOS
- 1.8 V main supply
- Parts
  - 9-stage ring oscillator
  - 3-stage ring oscillator
  - Integrated LC oscillator
  - Charge-pump circuits
  - PFD networks
- MOSIS SCMOS rules for ring oscillators : 0.20 µm minimum drawn channel length

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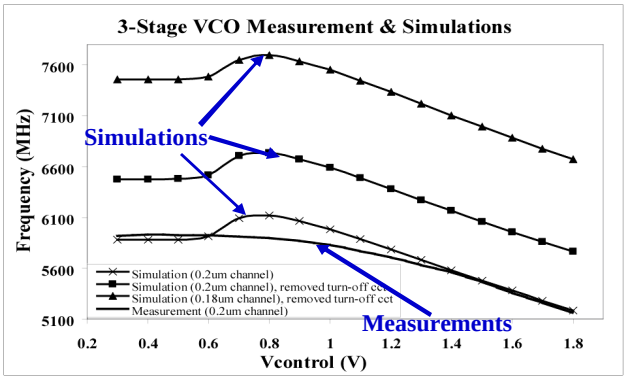
Three-Stage Multiple-Pass Ring Oscillator



- Simulations : 5.18-6.11 GHz
- Measurements : 5.16-5.93 GHz
- Linear characteristics
- Possible operation up to 7.7 GHz

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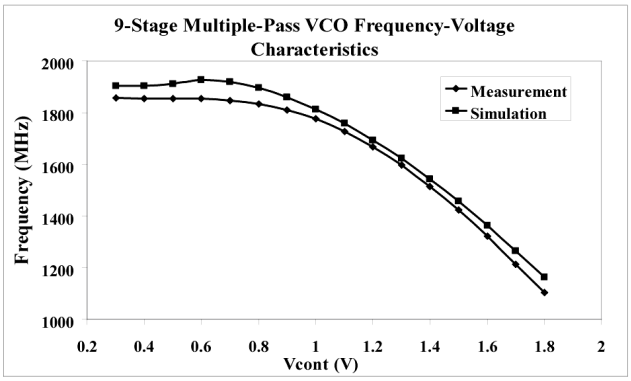
Nine-Stage Multiple-Pass Ring Oscillator



- Simulations : 1.16-1.93 GHz
- Measurements : 1.10-1.86 GHz
- Linear characteristics

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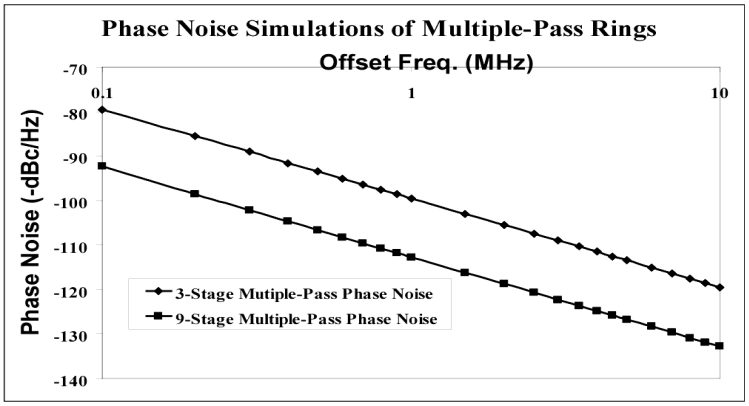
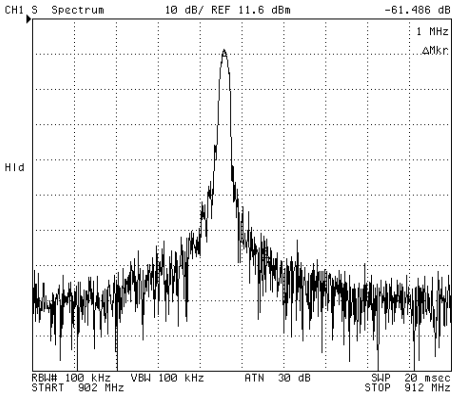
Phase Noise Simulations



- Spectre RF
- Models with thermal noise, no 1/f noise
- 3-stage : -99.5 dBc/Hz (f_{off} = 1 MHz, f_0 = 5.79 GHz)
- 9-stage : -112.8 dBc/Hz (f_{off} = 1 MHz, f_0 = 1.82 GHz)

Phase Noise Measurements

Power Spectrum at 1:2 Output of 9-Stage Ring



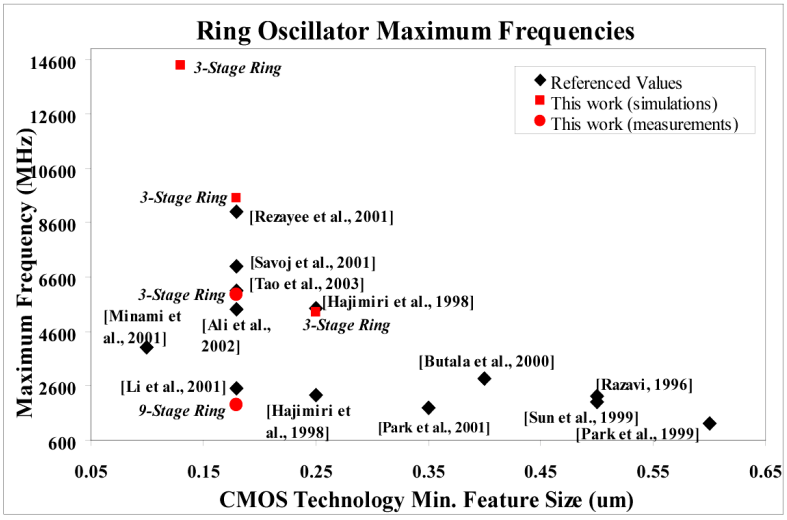
- Spectrum analyzer
- 9-Stage ring oscillator :
  - -105.5 dBc/Hz phase noise at (1MHz offset, 1.8 GHz center)

$$L\{\Delta w\} = SB_{meas} - 10\log(RBW) - 20\log(\Delta w / \Delta w_{meas}) + 20\log(w_0 / w_{meas})$$

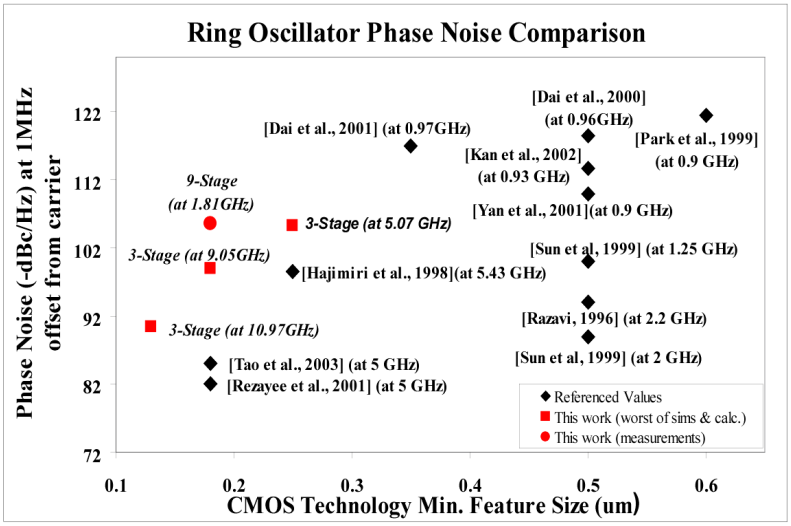
- Larger result due to power-supply/ground noise + 1/f noise
- Low frequency noise

Performance Comparison

Frequency Performance Comparison



Phase Noise Performance Comparison



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Applications

Possible Applications

- CPU, DSP, DRAM clock generation
- System synchronization (deskewing) : Zero delay clock buffers
- Oversampling A/D converters
- Wired transceivers
  - Gigabit Ethernet
  - 10 Gigabit Ethernet (IEEE 802.3ae)
  - SONET, STS-192[1], STS-96, STS-48, STS-36, STS-24, STS-18,…

Need LC Oscillators

- Wired transceivers
  - SONET, STS-768[2]
- Wireless transceivers
  - Bluetooth[3] (power)
  - HomeRF[4] (power)
  - Wireless LAN (IEEE 802.11a)[5]
  - HiperLAN
  - GSM[6]
  - DECT[7]

[1] [Mukherjee at al., 2002] : at 10 GHz, -90 dBc/Hz at a 1 MHz offset is required for a loop bandwidth of 10 MHz.

[2] ~40 GHz operation frequency required (for serial transmission)

[3] at 2.44 GHz, -119 dBc/Hz is required at 3 MHz offset

[4] at 2.404-2.478 GHz, -77 dBc/Hz is required at 3 MHz offset

[5] at 5.15-5.35 GHz, -110 dBc/Hz is required at a 1 MHz offset

[6] at 0.9/1.8 GHz, -138/-145 dBc/Hz is required at 3 MHz offset

[7] at 2.4 GHz, -134 dBc/Hz is required at 5.128 MHz offset

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Summary and Conclusions

- Ring oscillator analysis (time, s-domain)
- How to improve characteristics of ring oscillators
- Multiple-pass architecture with latching saturated stages for high frequency, low-noise in CMOS
- Estimations :
  - Up to 9.5 GHz in 0.18 µm CMOS, -99.2 dBc/Hz Phase Noise
  - Up to 14 GHz in 0.13 µm CMOS, -90.5 dBc/Hz Phase Noise
- Suggestion of practical applications
- Results suggest that it is not always necessary to resort to integrated LC networks for high-frequency low-noise VCO/CCO modules

Questions

?