Lecture 190 – All Digital Frequency Synthesizer for Bluetooth

What is bluetooth?

- A short-range technology for integration into mobile and handheld devices that is targeted to replace cables.
- Radio specification
  - Frequency range: 2400 ~ 2483.5 MHz
  - Spectrum spreading: FHSS (Frequency Hopping Spectrum Spreading)
    - $f_k = 2.402 + k$ MHz, k = 0, …, 78 (dwell time: .625 ms)
    - Channel bandwidth: 1 MHz
  - Modulation: GFSK (BT = 0.5; 0.28 < h < 0.35)
  - Receiver sensitivity: -70 dBm @ 0.1% BER
  - Coverage area: Up to 10 m
  - Transmit power: 0 dbm (up to 20 dbm with power control)

Frequency synthesizer specification for bluetooth application

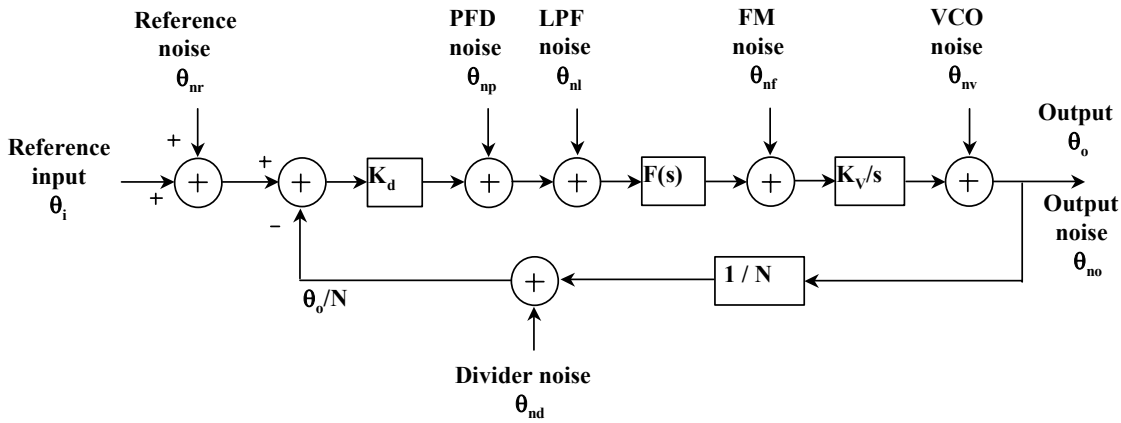
- Frequency range: 2.402 ~ 2.480 GHz
- Settling time ≤ 220 usec
- Phase noise ≤ - 89 dBc/Hz @ 500 KHz offset
  ≤ - 121 dBc/Hz @ 2 MHz offset
- Channel bandwidth: 1 MHz, Error tolerance: ± 20 ppm (96 KHz)

Architecture selection

- Direct digital frequency synthesizer: limit of speed by Nyquist sampling theorem
- Integer-N frequency synthesizer (Channel spacing = reference freq.)
  - Channel spacing ↑ Divide ratio ↑ In-band phase noise ↑
  - Channel spacing ↑ Loop bandwidth ↓ Switching time ↑
- Fractional-N frequency synthesizer (Channel spacing « reference freq.)
  - Lower in-band noise
  - Faster lock
  - Fractional spurs eliminated by modulating divide ratio using high-order ∑Δ modulator

System level design using linear model

- When PLL is in lock state, the linear model can be used to analyze it.
- Reference signal frequency » Loop bandwidth ⇒ Continuous model



$$B(s)=\frac{\theta_o(s)}{\theta_i(s)}=\frac{G(s)}{1+G(s)H(s)},\ \text{where}\ G(s)=\frac{K_dK_vF(s)}{s}\ \text{and}\ H(s)=\frac{1}{N}$$

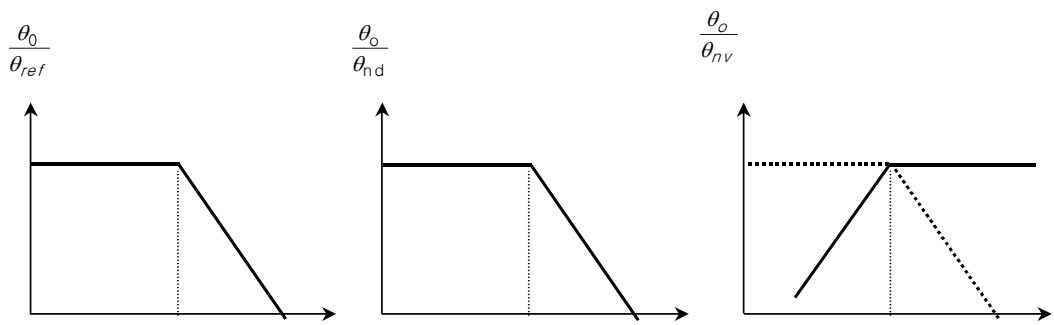
- Output noise power, θ_{no}

$$\theta_{no}^2 = N^2\left(\theta_{nr}^2+\theta_{n,eq}^2\right)\cdot\left(\frac{O(s)}{1+O(s)}\right)^2+\theta_{nv}^2\left(\frac{1}{1+O(s)}\right)^2$$

Low-pass transfer function — High-pass transfer function

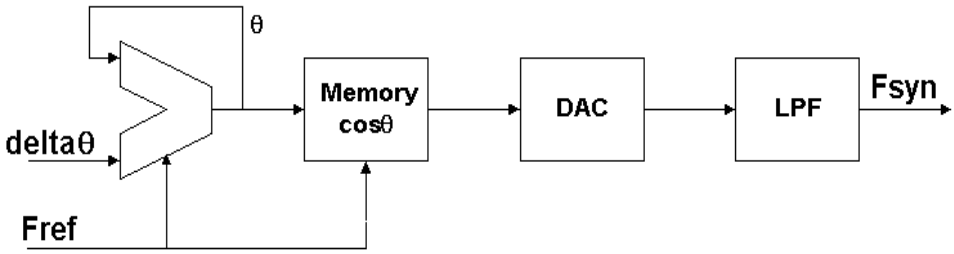
$$\text{where}\ \theta_{n,eq}^2=\frac{1}{K_d^2}\left(\theta_{np}^2+\theta_{nl}^2\right)+\frac{1}{K_d^2F(s)^2}\theta_{nf}^2+\theta_{nd}^2\ \text{and}\ O(s)=G(s)\cdot H(s)=\frac{K_dK_vF(s)}{sN}.$$

- Reference noise and VCO inherent noise are the two major sources of phase noise in a PLL



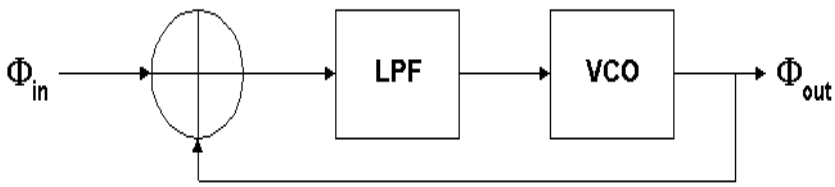
Direct Digital Frequency Synthesizer

- Direct Digital Frequency Synthesizer (DDFS)
  - Advantage: high frequency resolution, fast switching time
  - Disadvantage: high power consumption, limitation of highest frequency by Nyquist sampling theorem, discrete narrow band spurious signals
- The DDFS methods are combined with PLLs to achieve fine frequency steps with reasonable phase noise



PLL Based Frequency Synthesizer

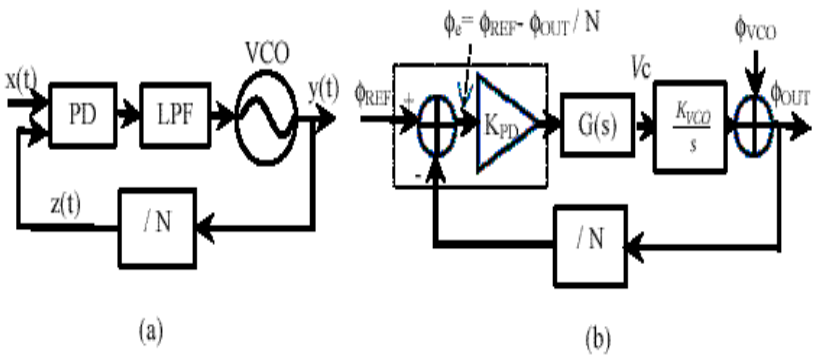
- PLL is negative feedback system whose output frequency is locked onto an input signal
  - PD: error amplifier
  - LPF: suppress high frequency component of PD
  - VCO: Voltage Controlled Oscillator
- Low cost and good spurious suppression
- Coarse frequency resolution or frequency step and bad phase noise
- Slow switching speed for negative feedback loop



PLL Based Frequency Synthesizer (continued)

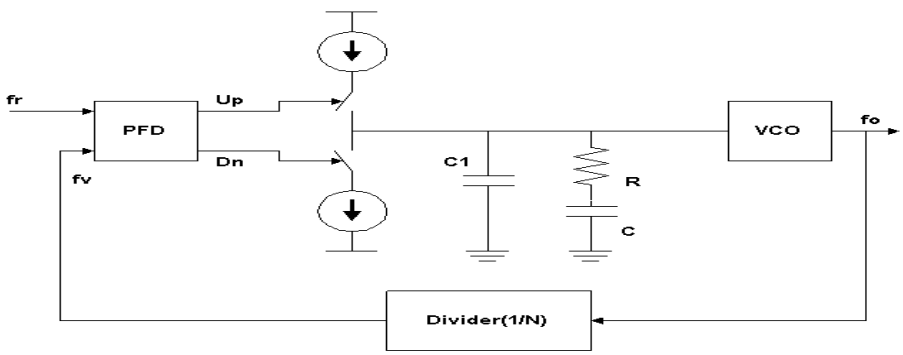
- Closed loop transfer function

$$B(s)=\frac{A(s)}{1+A(s)\cdot\beta(s)}=\frac{K_{PD}\cdot K_{VCO}\cdot G(s)/s}{1+K_{PD}\cdot K_{VCO}\cdot G(s)/N\cdot s}=\frac{N\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}$$



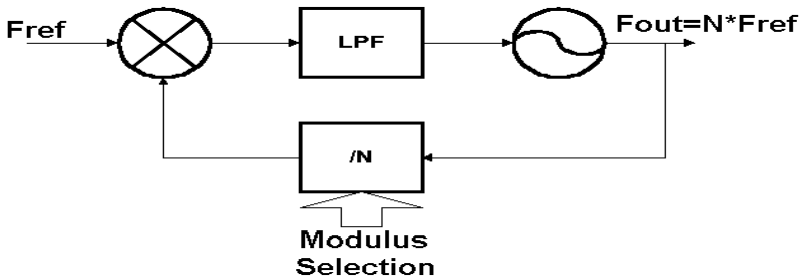
Charge-Pump Frequency Synthesizer

- Charge-pump phase locked loop (type 2, 3rd order PLL)
  - Advantage: low phase noise
  - Disadvantage: process dependency, slow locking speed, large passive external elements (Rs and Cs)



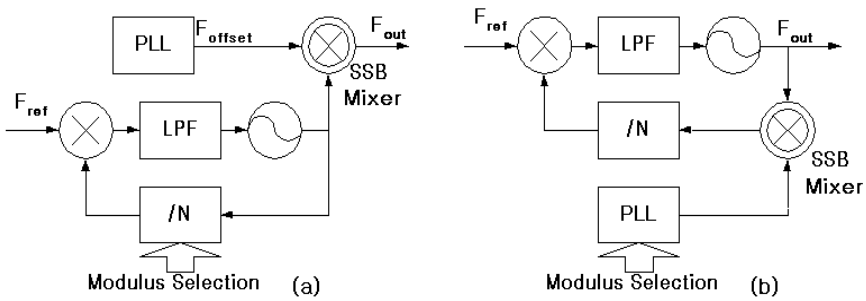
Integer-N Frequency Synthesizer

- Integer-N Frequency Synthesizer
  - $f_{out}=N \cdot f_{ref}$, N: integer number
  - Frequency step size= reference frequency
  - Inverse relationship between step size and phase noise
  - To achieve a small channel spacing → a low f_{ref} → narrow loop BW → increasing the settling time, and reducing VCO noise suppression
  - Low reference → large integer N → increasing in-band phase noise



Dual Loop Frequency Synthesizer

- Dual Loop Frequency Synthesizer
  - Mixer is incorporated into the PLL → alter the relationship between the channel spacing and the reference frequency of integer N synthesizer
  - 2 dual loop types: combination of 2 PLLs by a single side band mixer in parallel and in series
  - Adding fixed high offset frequency and low variable frequency



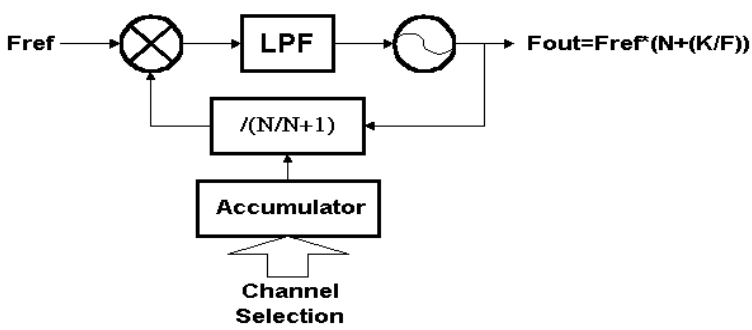
Dual Loop Frequency Synthesizer

- Dual Loop Frequency Synthesizer
  - Parallel configuration: (a fixed frequency + changeable frequency) @the output → large spurs during mixing
  - Series configuration: changeable frequency is added inside the loop → longer time to settle, small sideband from the mixer
  - The loop BW of the high frequency loop can be large→ more reduction of phase noise close to the carrier
  - The division number of the divider can be reduced ← fixed offset frequency
  - The sidebands produced from non-ideal SSB mixing and larger power consumption

Fractional-N Frequency Synthesizer

- Fractional-N Frequency Synthesizer
  - Doesn't require more current, complexity or bigger dies
  - The reference fref >> frequency step time, fstep
  - $f_{VCO} = f_{ref}(N+(K/F))$

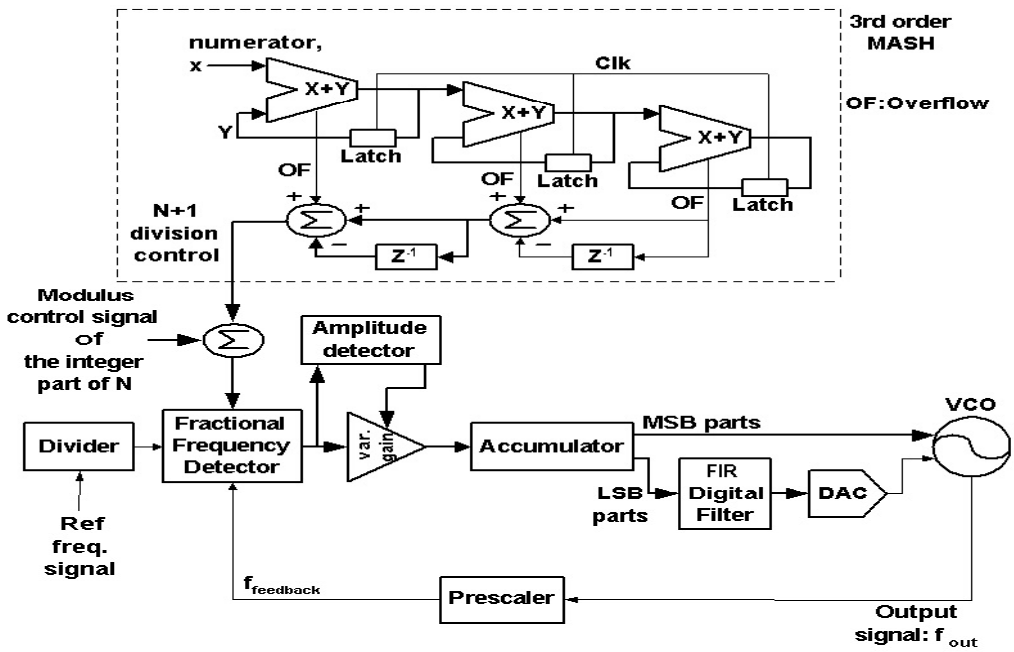
$$N_{fractional} = \frac{N\cdot(F-K)+(N+1)\cdot K}{F} = N+\frac{K}{F}, F \geq K \geq 0$$



All Digital Frequency Synthesizer

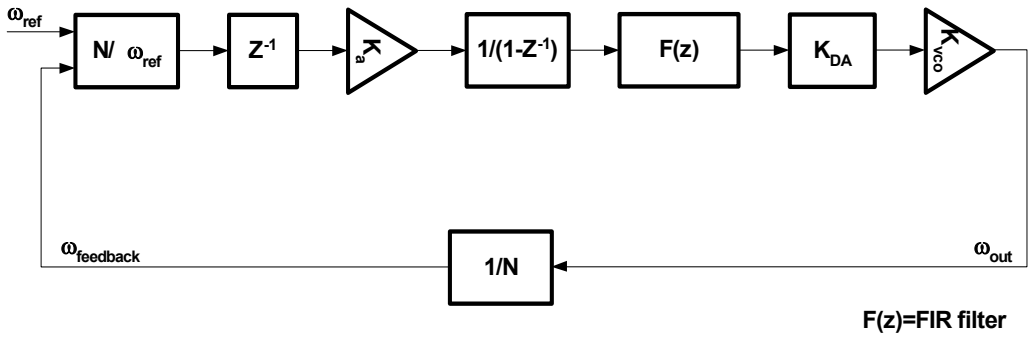
- Apply digital filter to achieve a single-chip freq. synthesizer
  - Fully-integrated freq. synthesizer
  - Easy to implement Multi-mode application (ex. W-CDMA/GPRS/GSM)
  - Increase design robustness
- Apply MASH
  - Reduced spurs
  - Fast locking time
- Apply switched-current Oscillator
  - Wide locking range
  - Fast locking time

Block diagram

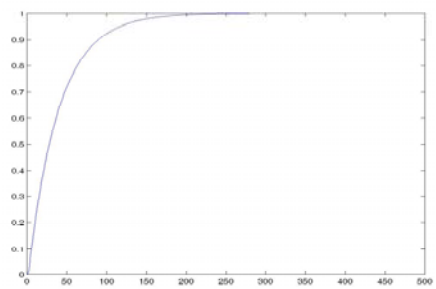


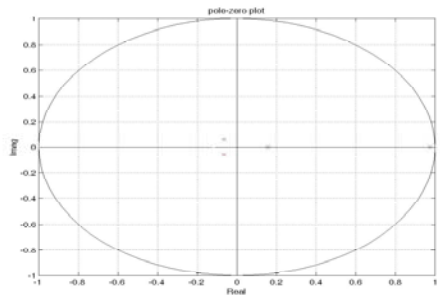
Linear model of the proposed freq. syn.

$$H(z)=\frac{\omega_{feedback}}{\omega_{ref}}=\frac{K\cdot F(z)\cdot z^{-1}}{1-z^{-1}(1-K\cdot F(z))},K=\frac{K_{DA}\cdot K_{VCO}\cdot K_a}{\omega_{ref}}$$

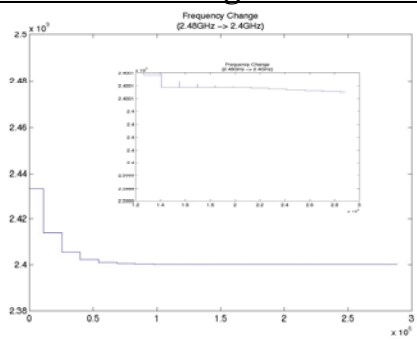


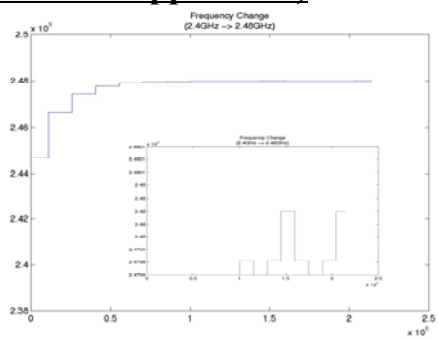
System level unit step response and pole-zero plot



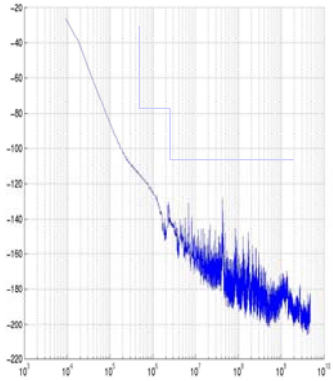


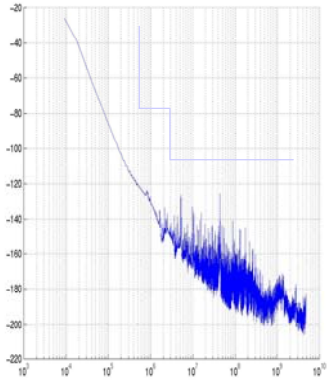
System level locking time simulation (Bluetooth application)





System level noise simulation (Bluetooth application)

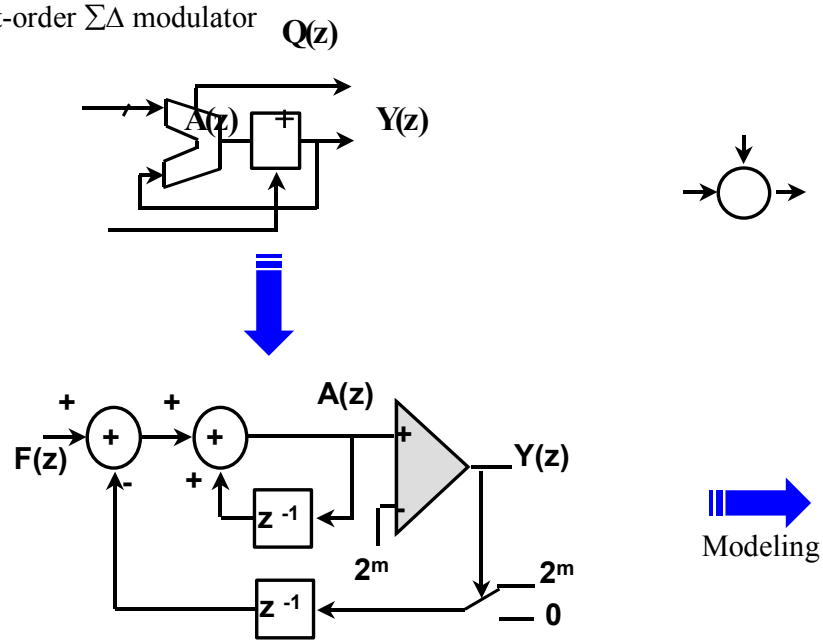


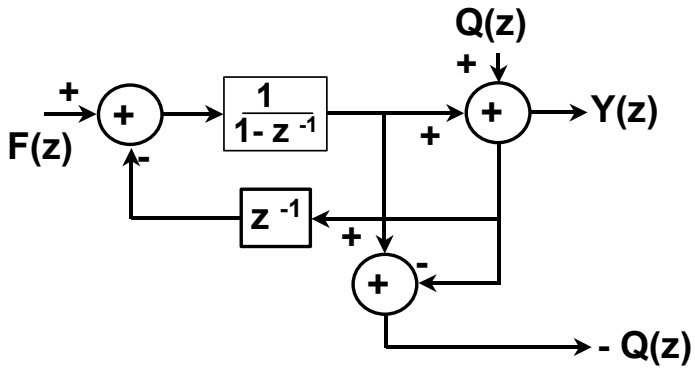


$Fractional = Num/Den =$ 32/64 0/64

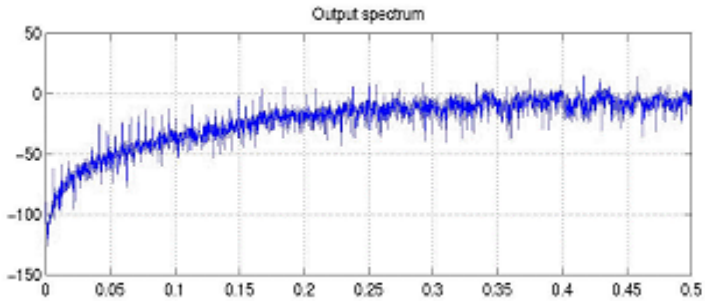
Block design: High-order ∑Δ Modulator

- Used to eliminate fractional spurs by modulating divide ratio
- Higher-order modulator is used to meet higher spurs specification
- First-order ∑Δ modulator





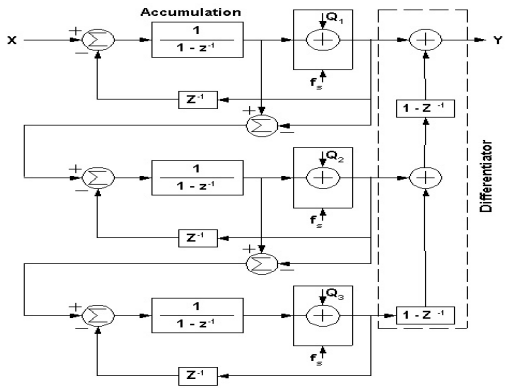
- Third-order ∑Δ modulator system-level simulation result

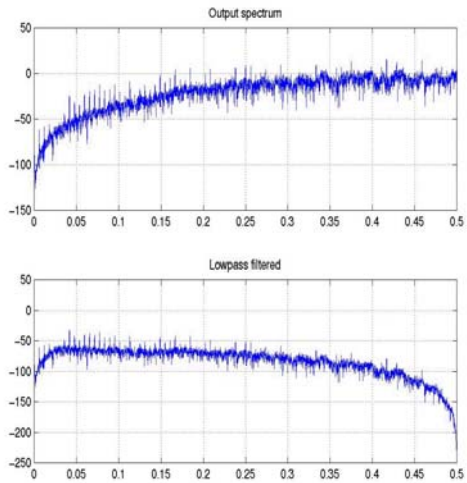


Block Design (continued):

- 3rd order MASH system level simulation

$$y(z) = x(z) + (1 - z^{-1})^3 q_3(z)$$
$$y(z) = x(z) + H_{noise}(z) q_3(z)$$

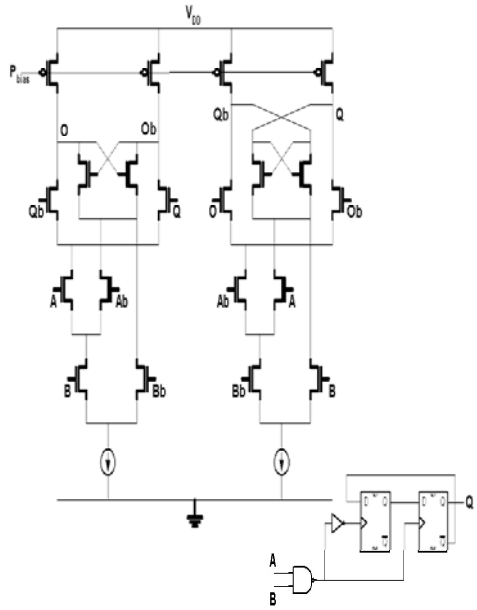




Block Design (continued)

- Conventional CMOS static logic
  - Wide noise margins
  - High packaging density
  - Zero static-power-dissipation
  - Coupling between the analog blocks and the digital blocks
  - Susceptible to power-supply noise

- Current Mode Logic
  - Constant current source
  - Differential input & output



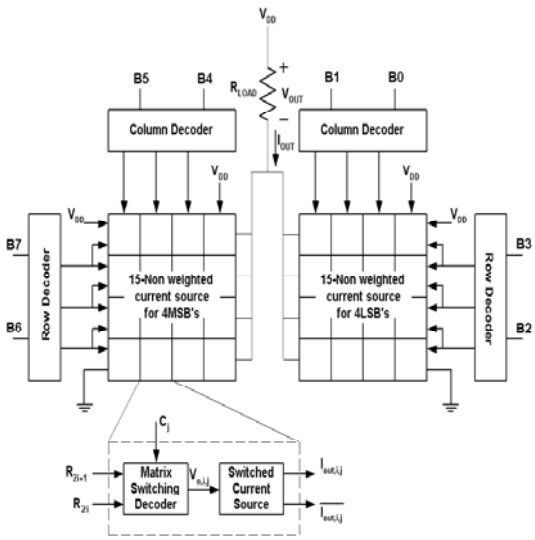
Block Design (continued)

- 8-bit Digital-to-Analog Converter
  - Symmetric 2-stage current-cell matrix architecture
  - A 4-MSB current-cell matrix and a 4-LSB current-cell matrix
  - Use thermometer-code
  - Monotonic conversion characteristic

$$I_{out} = \begin{aligned} &I_{MSB}(2^3 B_7 + 2^2 B_6 + 2^1 B_5 + 2^0 B_4) + \\ &I_{LSB}(2^3 B_3 + 2^2 B_2 + 2^1 B_1 + 2^0 B_0) \end{aligned}$$

$$I_{MSB} = 16 \cdot I_{LSB}$$

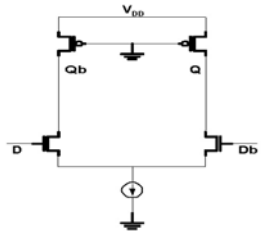
$$V_{out} = I_{out} \cdot R_{LOAD}$$



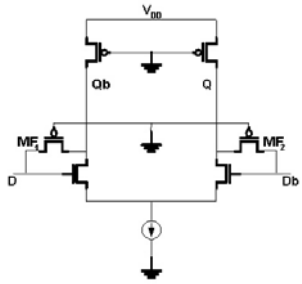
Block Design (continued)

- Prescaler: high operating frequency, low power dissipation, low phase-noise contribution
- Feedback CML: Transistors, MF_1 and MF_2

$$A(f)=\frac{A_d(f)}{1+F_b\cdot A_d(f)}=\frac{A_d(0)}{1+F_b\cdot A_d(0)}\cdot\frac{1}{1-j(\frac{\omega}{\omega_p})(\frac{1}{1+F_bA_d(0)})}$$

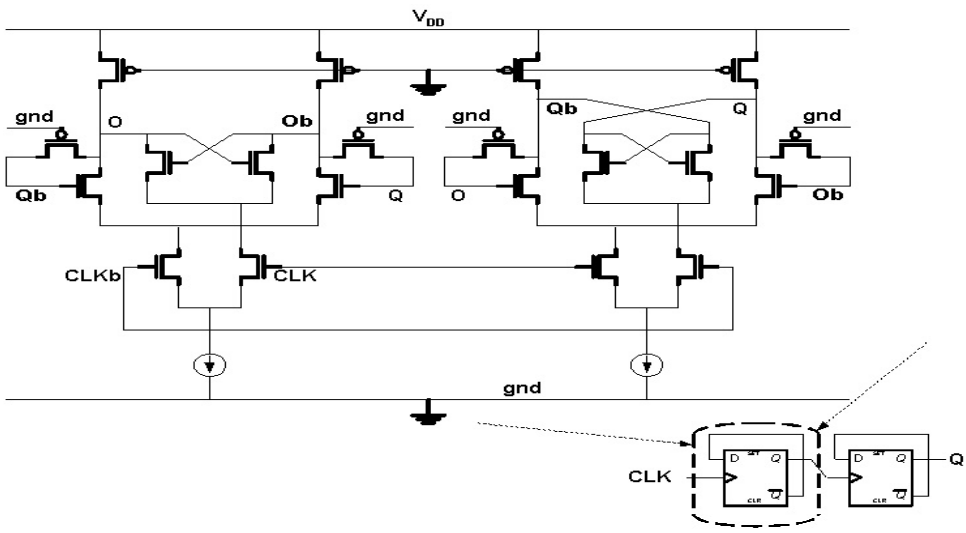


- F_b: the gain of the feedback transistors
- The BW of the feedback CML is wider than the BW of the conventional CML



Block Design (Continued)

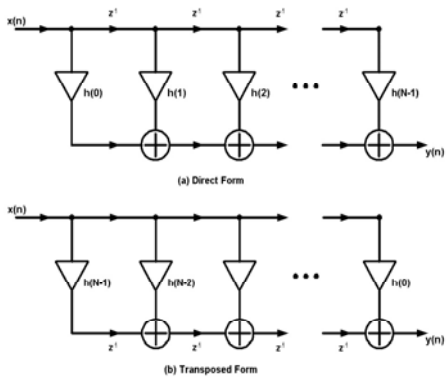
- Feedback Current Mode Logic in D Flip-Flop

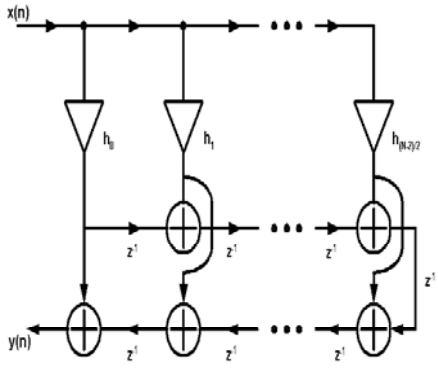


Block Design (Continued)

- FIR digital filter

(a) Single flow graph of nth order (b) Linear Phase transpose direct form





- Floating point coefficient

