LECTURE 210 – CLOCK AND DATA RECOVERY CIRCUITS - II

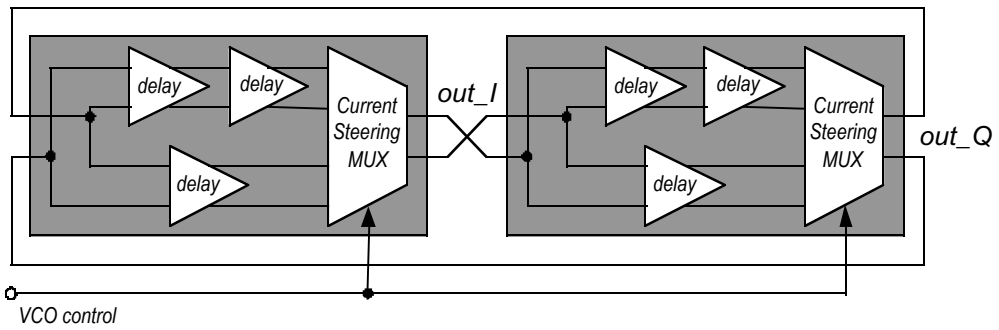
(References [6])

VOLTAGE CONTROLLED OSCILLATORS FOR CDR APPLICATIONS

Comparison of VCOs

Comparison of VCO Topologies				
	Relaxation	Ring	LC	Quadrature LC
Control Voltage	Differential ↑	Differential ↑	Single-ended ↓	Differential ↑
Phase Noise	High ↓	High ↓	Low ↑	Moderate
Tuning Range	Wide ↑	Wide ↑	Narrow ↓	Medium
VCO Gain	High ↓	High ↓	Low ↑	Medium
PVT Variations	High ↓	High ↓	Low ↑	Low ↑

Ring Oscillator Example†

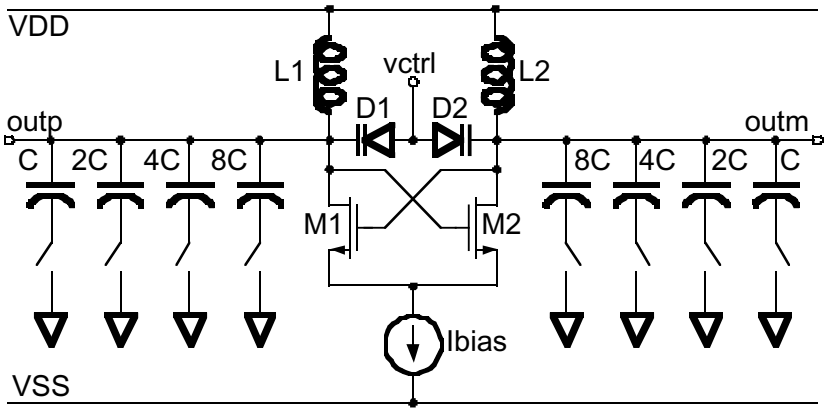


Comments:

- Tuning can be split into fine and coarse control
- Very wide tuning range
- Differential control
- Moderate phase noise

† R. Walker, *ISSCC*'1997, pp. 246-247.

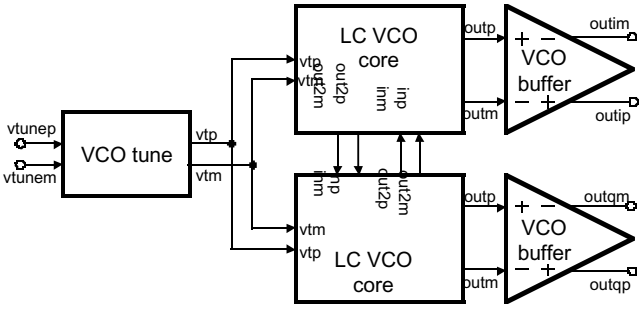
LC VCO Example



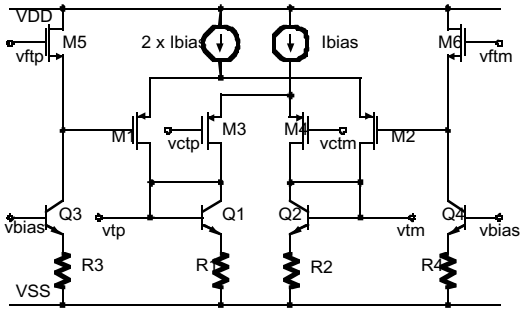
Comments:

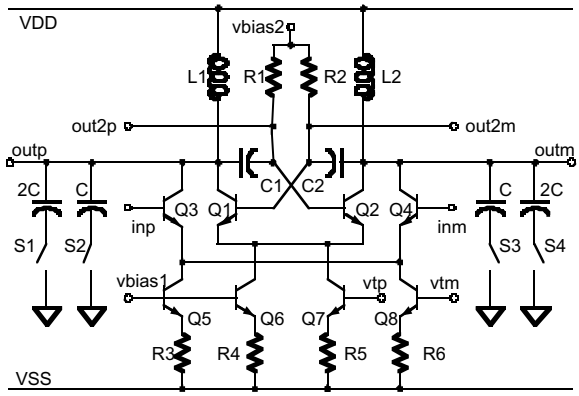
- Fine tuning is through varactor control
- Coarse tuning is achieved by binary weighted capacitor array
- Low tuning range
- Single-ended control
- Very good phase noise characteristics

Quadrature LC VCO Example



T.P. Liu, *IEEE VLSI* 1999, pp. 55-56





A.L. Coban, et. al., *VLSI* 2001, pp. 119-120

- Two identical LC VCOs are coupled in quadrature.
- VCO tuning is achieved through:
  - Adjusting the coupling between the two oscillator cores
  - Changing the LC-tank capacitance

A Design Procedure for VCOs for CDR Applications

The following procedure seeks to maximize the tuning range and minimize the phase noise with the knowledge of four parameters:

- Load capacitance, C_L
- Required output voltage swing
- Center frequency, f_o
- Power

The first two parameters may require a buffer as shown below.

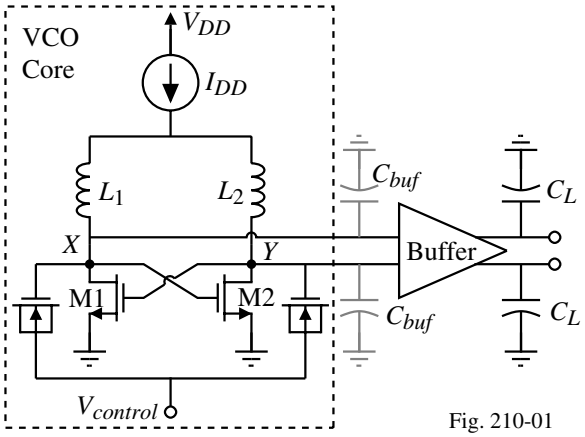


Fig. 210-01

Design Procedure for VCOs – Continued

Other circuits that the VCO may have to drive include a flip-flop in a divider chain, two flipflops in the demultiplexer and a 50Ω output driver:

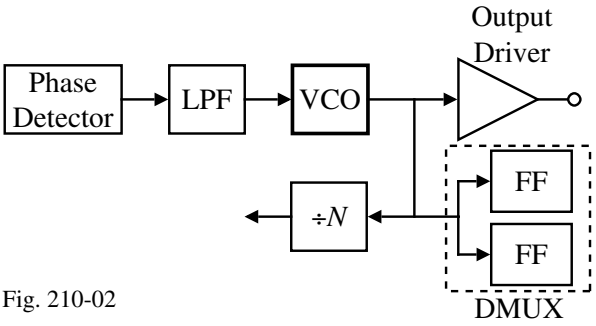


Fig. 210-02

Procedure:

1.) With the power budget and hence the value of I_{DD} the width of M1 and M2 is chosen to yield an average CM level of approximately $0.5V_{DD}$ at the X and Y nodes. Note that when $V_X = V_Y$, that $V_{DG1} = V_{DG2} = 0$.

$$I_D = \frac{K'W}{2L}(V_{GS}\text{-}V_T)^2\text{: } V_{GS} = 0.5V_{DD} \text{ and } I_{DD} \quad \rightarrow \quad \frac{W}{L} \quad \rightarrow \quad g_m$$

2.) Design the inductors, L_1 and L_2. To maximize the tuning range (and Q) the inductance must be minimized. To get the oscillator to start-up, the following must hold:

$$(g_m R_{p,min})^2 = 1$$

However, $R_{p,min}$, is the parallel resistance of the tank and is primarily due to the inductor.

$$R_{p,min} \approx QL_{min}\omega_{osc} \quad \rightarrow \quad (g_m\, QL_{min}\omega_{osc})^2 = 1 \quad \rightarrow \quad L_{min} = \frac{1}{g_m Q \omega_{osc}}$$

The above assumes that the Q is approximately constant with the value of L_{min}.

VCO Design Procedure – Continued

3.) With $L = L_{min}$, the oscillation amplitude is quite small in order to maintain unity loop gain. If the amplitude grows, the transistor nonlinearities reduce the loop gain which may prevent full swing. One must also be careful of the variation of g_m and Q with PVT corners possibly prohibiting oscillation at some corners. Therefore, the values of L and R_p must sufficiently exceed L_{min} and $R_{p,min}$ to provide the required voltage swings and start under worst case conditions.

4.) The value of R_p can be related to the required output swing as follows. M1 and M2 each have an average current of $0.5I_{DD}$. If the drain currents are approximated by sinusoids varying between I_{DD} and zero, the V_X and V_Y swing from $0.5V_{DD}$-$I_{DD}R_p$ and $0.5V_{DD}$+$I_{DD}R_p$. For this voltage sinusoid, the largest peak voltage is $0.5V_{DD}$=$I_{DD}R_p$ giving

$$R_{p,swing} = \frac{V_{DD}}{2I_{DD}} \quad \text{(minimum parallel tank resistance giving maximum swing)}$$

$$\therefore \quad L_{opt} = \frac{V_{DD}}{2I_{DD}} \cdot \frac{1}{Q\omega_{osc}}$$

5.) With W/L and L_{opt} known, the varactor capacitance can be found as

$$C_{tot} = \frac{1}{\omega_{osc}^2 L_{opt}}$$

where $C_{tot} = C_{var} + C_{gs} + C_{bds} + 4C_{gd} + C_{inductor} + C_{buffer}$

Designing a VCO for CDR Applications

Use the above procedure to design a VCO for 5GHz using 0.18μm CMOS technology having $K_N' = 120\mu A/V^2$ and $V_{TN} = 0.5V$. Assume the Q of the inductor is 5, $V_{DD} = 1.8V$ and the power is to be 5mW. Assume that $C_{gs} + C_{bds} + 4C_{gd} = 300fF$, $C_{inductor} = 50fF$, and $C_{buffer} = 200fF$.

Solution

1.) From the specifications we get $I_{DD} = 5mW/1.8V = 2.78mA$. The W/L can be found as,

$$\frac{W}{L} = \frac{I_{DD}}{K_N'(0.5V_{DD}\text{-}V_{TN})^2} = \frac{2.78mA}{0.12mA/V^2\,(0.9\text{-}0.5)^2} = 144.67 \approx 145$$

$$g_m = \sqrt{2K_N'\,(0.5I_{DD})145} = 6.95mS$$

2.) The minimum inductance can be found as

$$L_{min} = \frac{1}{g_m Q\omega_{osc}} = \frac{1}{6.95mS \cdot 5 \cdot 2\pi \cdot 5x10^9} = 0.916nH$$

3.) The value of R_p for maximum swing is

$$R_{p,swing} = \frac{V_{DD}}{2I_{DD}} = \frac{1.8}{2 \cdot 2.78mA} = 323.7\Omega$$

$$\therefore \quad L_{opt} = \frac{V_{DD}}{2I_{DD}} \cdot \frac{1}{Q\omega_{osc}} = 323.7\Omega \left(\frac{1}{5 \cdot 10\pi x10^9}\right) = 2.06nH$$

Example - Continued

4.) The value of C_{tot} is,

$$C_{tot} = \frac{1}{\omega_{osc}^2 L_{opt}} = \frac{1}{(10\pi \text{x} 10^9)^2 (2.06\text{nH})} = 491.6 \text{ fF}$$

Unfortunately, we see that $C_{var} = 491.6\text{fF} - 550\text{fF} = -58\text{fF}$

Our only choices are:

a.) Decrease the inductor size which will reduce the output swing.

b.) Decrease the buffer input capacitance which will degrade the drive capability.

c.) Decrease the W/L of the transistors by decreasing the power dissipation

5.) Since the inductance capacitance is small compared to the buffer input capacitance, we will choose to reduce the buffer input capacitance by a half giving

$$C_{var} = 491.6\text{fF} - 450\text{fF} = 42\text{fF}$$

A 2.5-GB/s CLOCK AND DATA RECOVERY CIRCUIT[†]

Introduction

Important considerations in this design are:

- Jitter
- VCO tuning range
- 2.5 GHz speed in 0.25μm CMOS technology
- Skew in phase detector and decision circuit

General block diagram of the architecture:

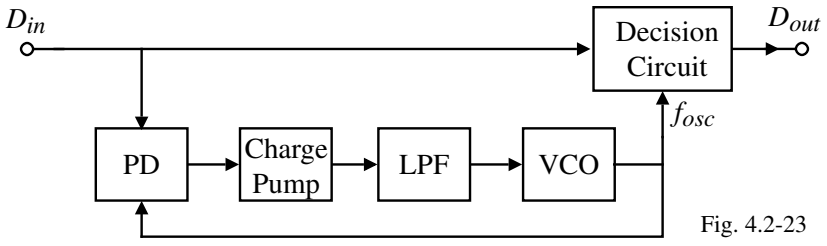


Fig. 4.2-23

[†] B. Razavi, "A 2.5-Gb/s 15-mW clock recovery circuit," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 472 - 480, April 1996.

Jitter Issues

Source of jitter:

- Input jitter, VCO device noise, VCO jitter due to ripple on control, supply and substrate noise.

Trade-offs in the choice of VCO gain, K_{VCO}:

- Low supply voltage necessitates high K_{VCO} for a given tuning range.
- For a given ripple on the control line, higher K_{VCO} results in higher jitter.

Solution:

Decompose the control line into fine and coarse control lines. The coarse control will be driven by the frequency detector and will remain quiet.

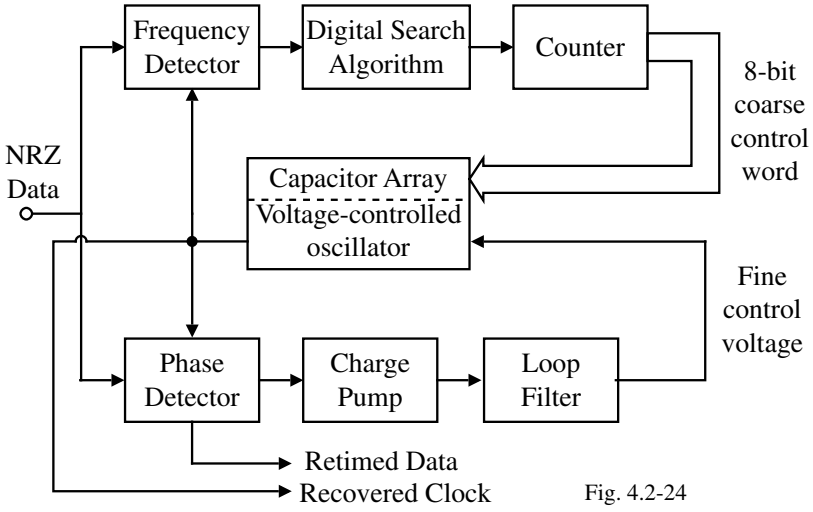


Fig. 4.2-24

Frequency Detector

Use the Pottbacker quadrature frequency detector:

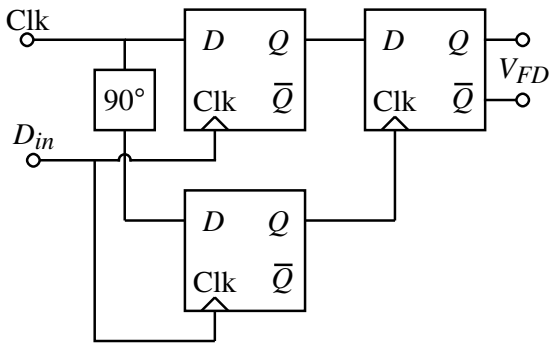
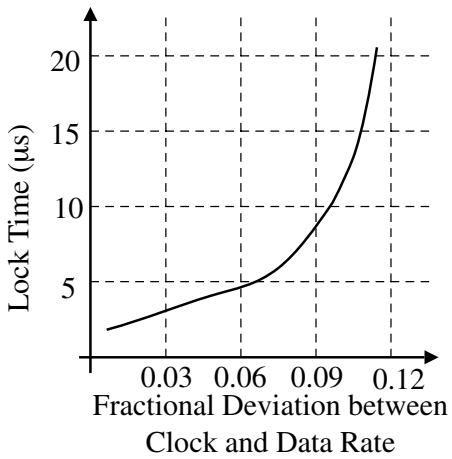


Fig. 4.2-25



Frequency Detector – Continued

Add a charge pump to the previous circuit to get:

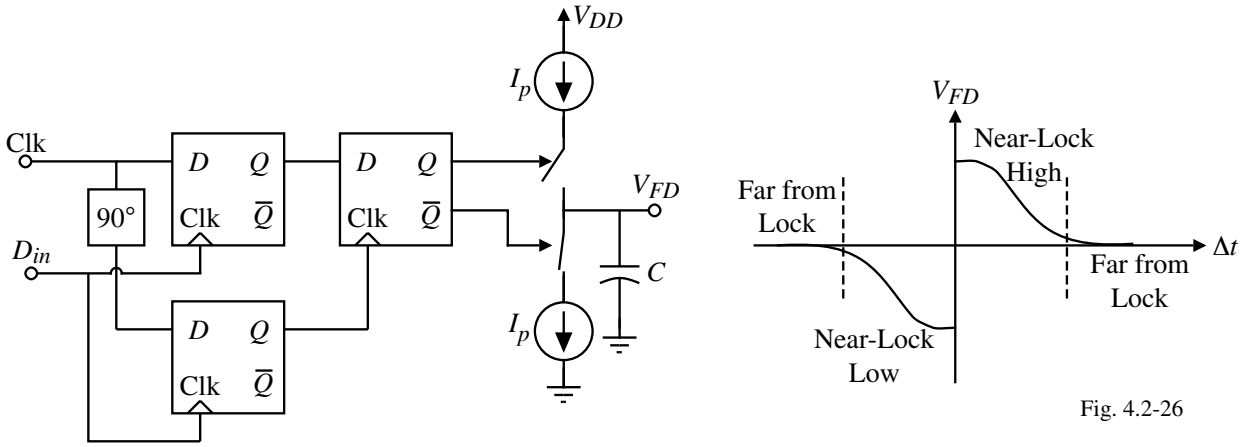


Fig. 4.2-26

Comments:

- In the near-lock regions, the output carries enough DC content to signify the polarity of the frequency difference.
- In the far-from-lock regions, the output carries little information.

Digital Search Algorithm with a Broad Range

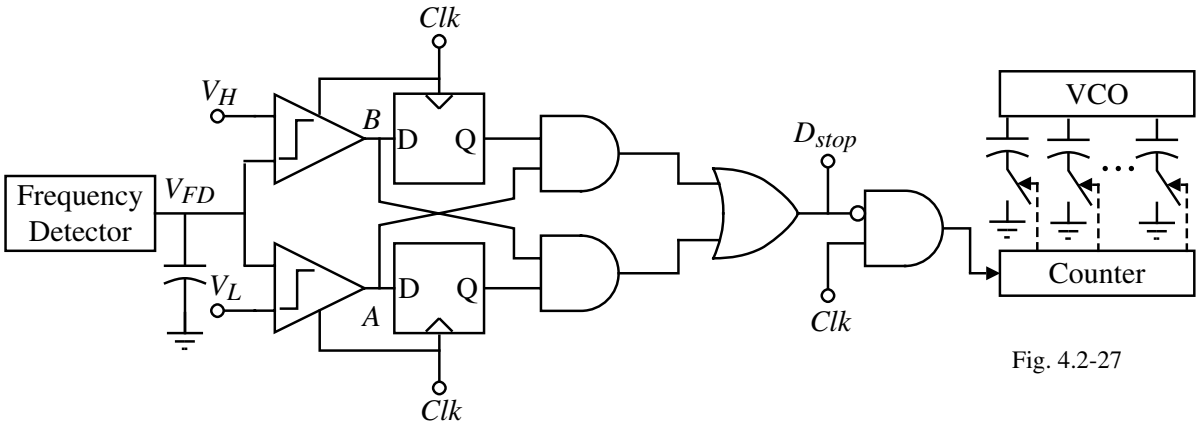


Fig. 4.2-27

Comments:

- 8 bits of resolution in the capacitor array allows a frequency step of 2.1 MHz.
- The fine VCO control can have a gain of only 50MHz/V.

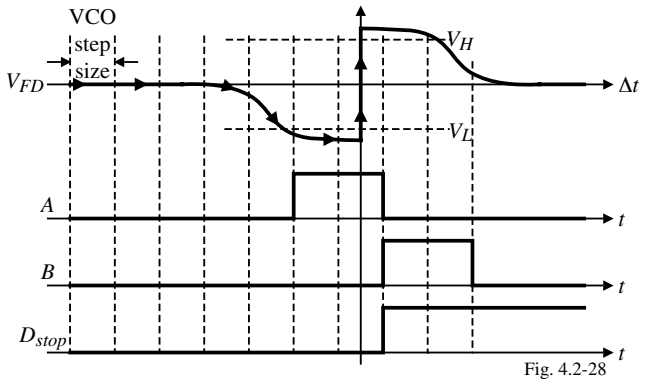


Fig. 4.2-28

VCO Circuit Implementation

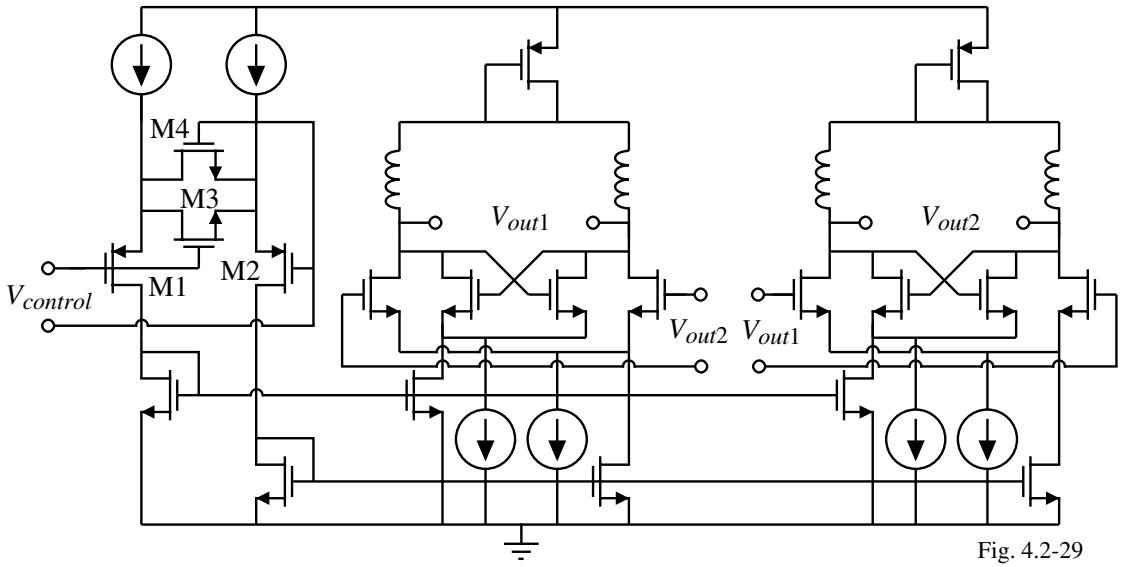


Fig. 4.2-29

Comments:

- Continuous frequency tuning is obtained by varying the coupling between oscillators.
- The VCO has a fully differential control.
- The input V/I converter, M1-M2, linearizes the input transconductance with M3-M4.

Capacitor Array

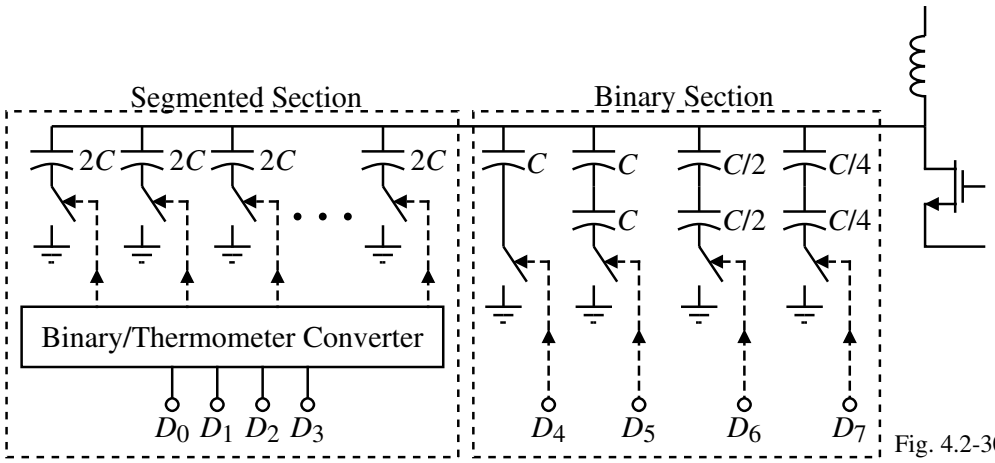


Fig. 4.2-30

Comments:

- The capacitors are divided into a 4-bit (MSB) segmented section and a 4-bit (LSB) binary-weighted section.
- Monotonicity guaranteed with up to 12.5% capacitor mismatch.
- Requires only 20 switched elements and has a worst case Q of 10.

Quadrature Frequency Detector Implementation

Use dummy loading to balance out delays.

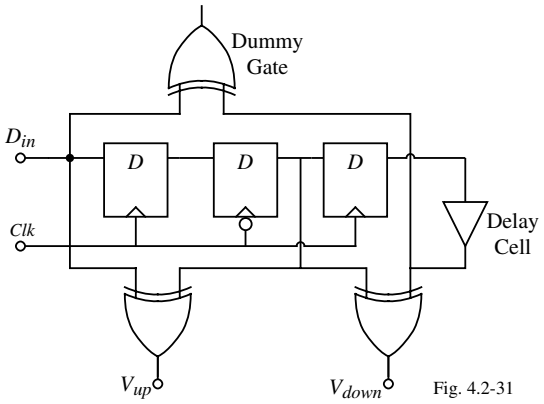
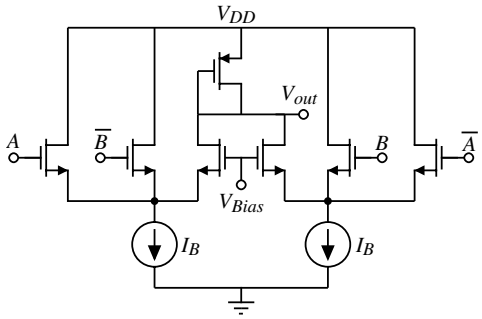


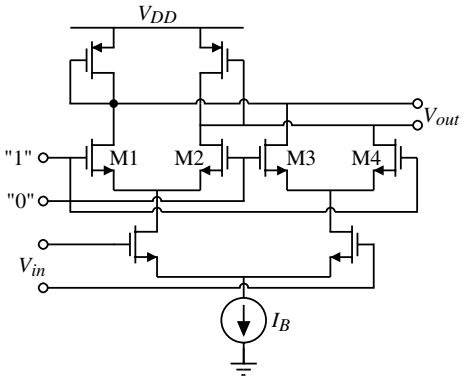
Fig. 4.2-31

Circuit Implementation:

Symmetric XOR

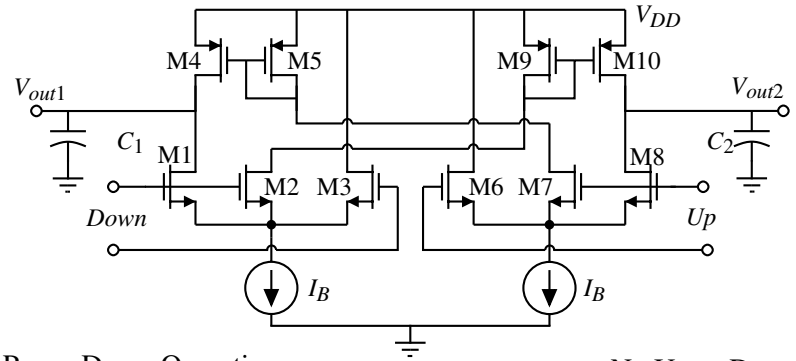


Delay Cell

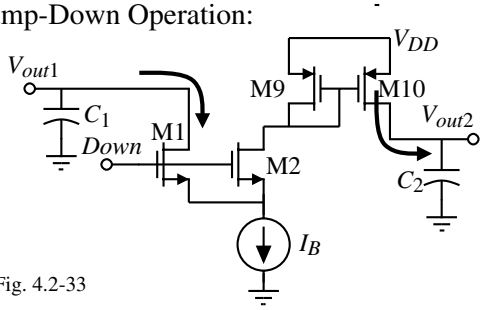


Charge Pump Implementation

Charge-Pump Circuit:



Pump-Down Operation:



No Up or Down Pulses:

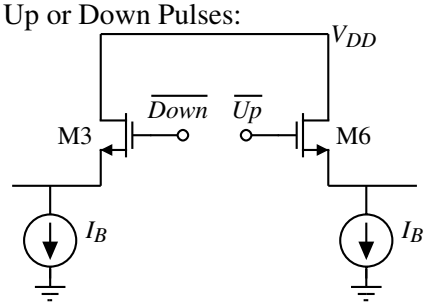


Fig. 4.2-33

This charge-pump has no current mismatch or charge mismatch.

Implementation of the Charge Pump – Continued

Conventional Implementation: This implementation:

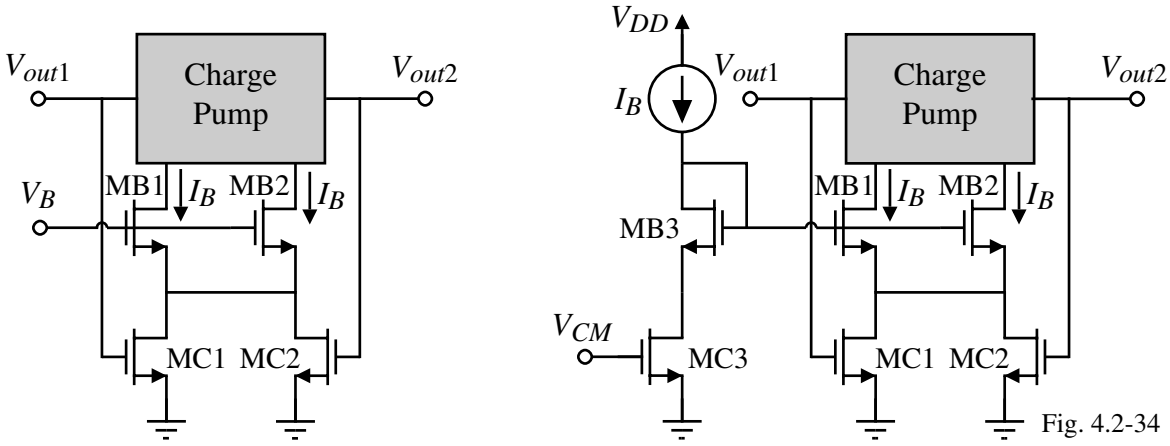


Fig. 4.2-34

The modified implemention stabilizes the common-mode output of the charge pump to a specific value, V_{CM}.

Theoretical Jitter Analysis (Open Loop)

Block diagram of the jitter model:

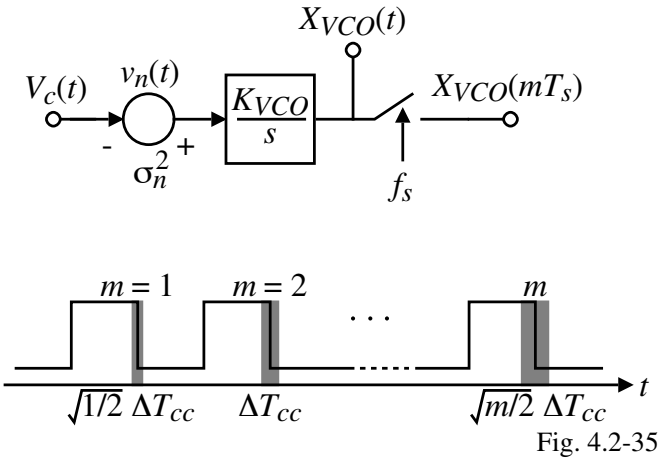


Fig. 4.2-35

The variation of the jitter as a function of mT_s can be written as,

$$\Delta T(mT_s) \approx K_{VCO}\sqrt{\frac{mT_s}{2}}\,\sigma_n\,\frac{T_s}{2\pi}$$

Therefore,

$$\Delta T(t) \approx \sqrt{\frac{f_o t}{2}}\;\Delta T_{cc}$$

Jitter Analysis – Continued

Recall that timing jitter creates phase noise, i.e.,

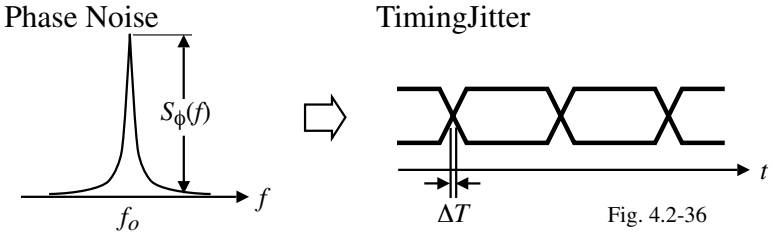


Fig. 4.2-36

$$S_\phi(f) \approx \frac{K_{VCO}^2\,\sigma_n^2}{2(2\pi)^2(f-f_o)^2}$$

$$\sigma_T^2 = \Delta T_{cc}^2 \approx \frac{2}{f_o^3} S_\phi(f)\,(f-f_o)^2$$

Illustration:

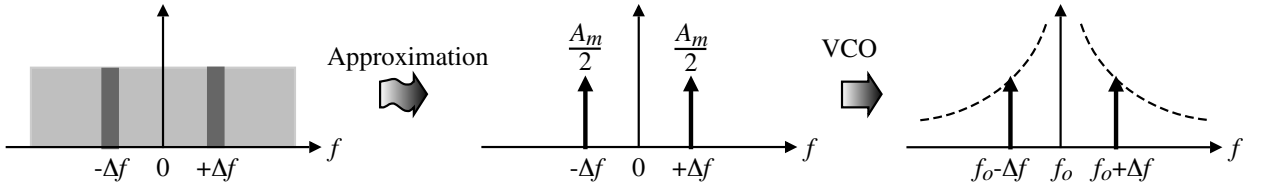


Fig. 4.2-37

Simulated Open- and Closed-Loop Jitter

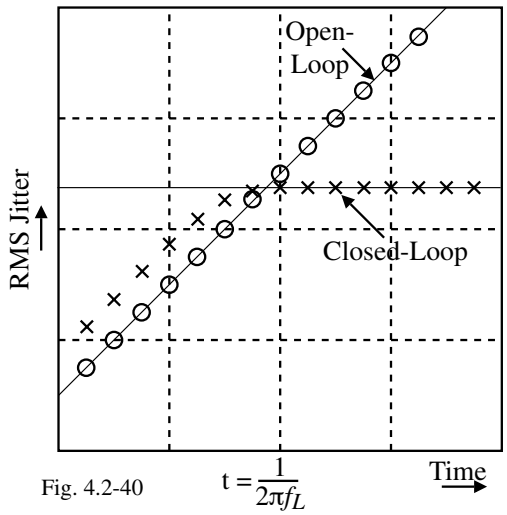
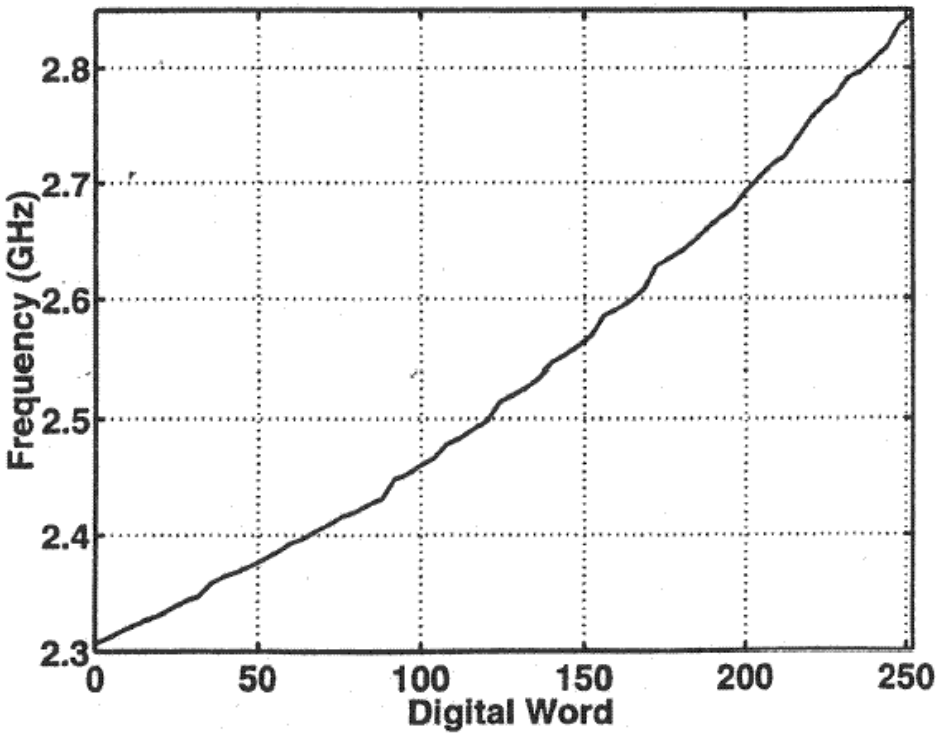


Fig. 4.2-40

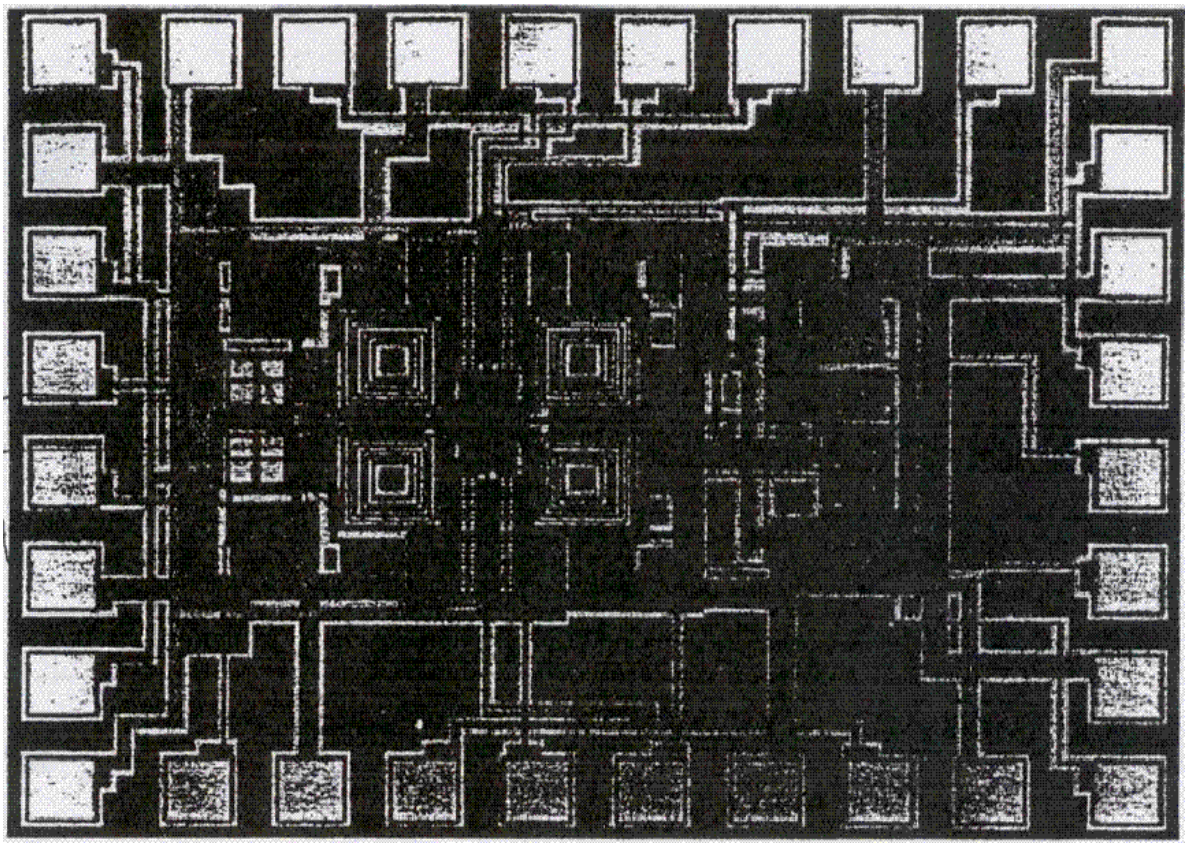
Maximum closed-loop jitter = $\sqrt{\frac{f_o}{2}}\;\Delta T_{cc}\sqrt{\frac{1}{2\pi f_L}}$

(J. McNeill, *JSSCC*, June 1997)

Measured VCO Characteristics

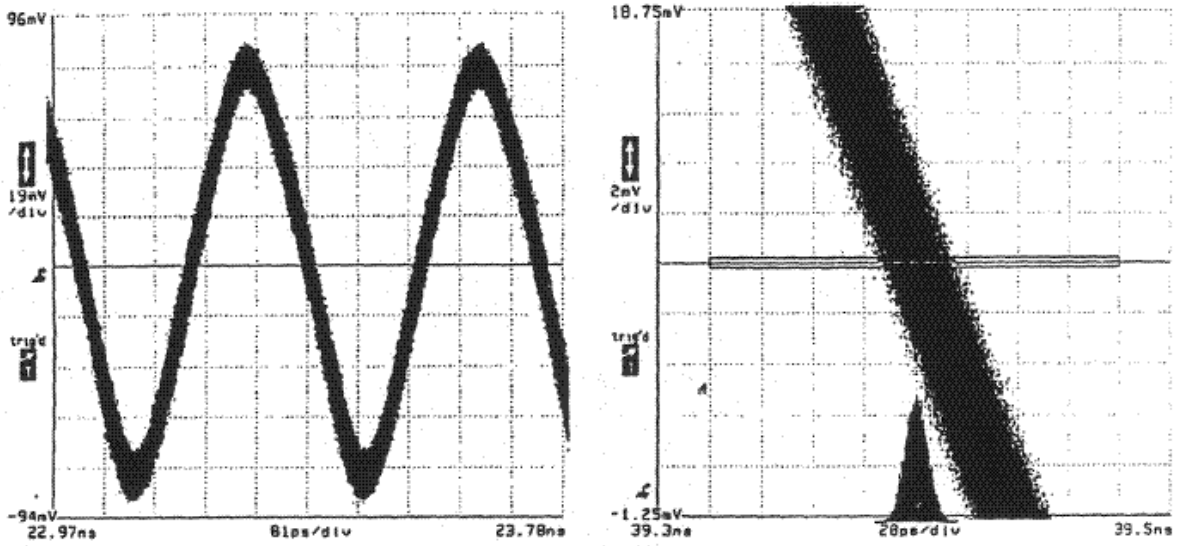


Chip Microphotograph



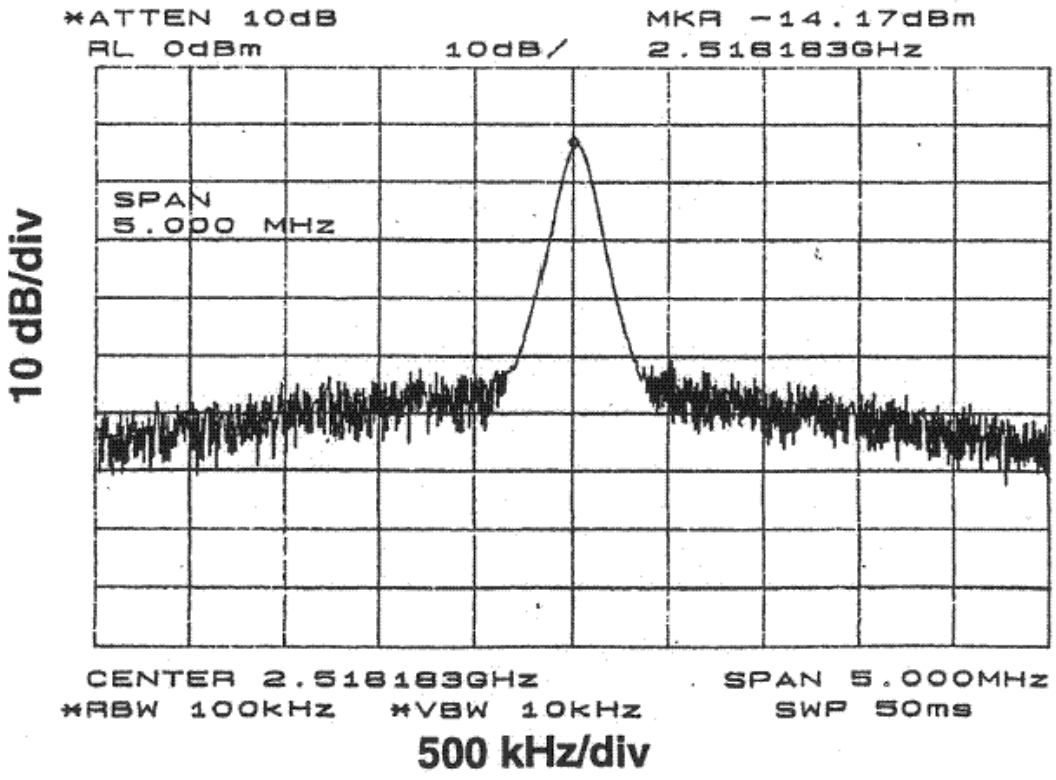
Jitter Measurements

PRBS of length 2^{23}-1:



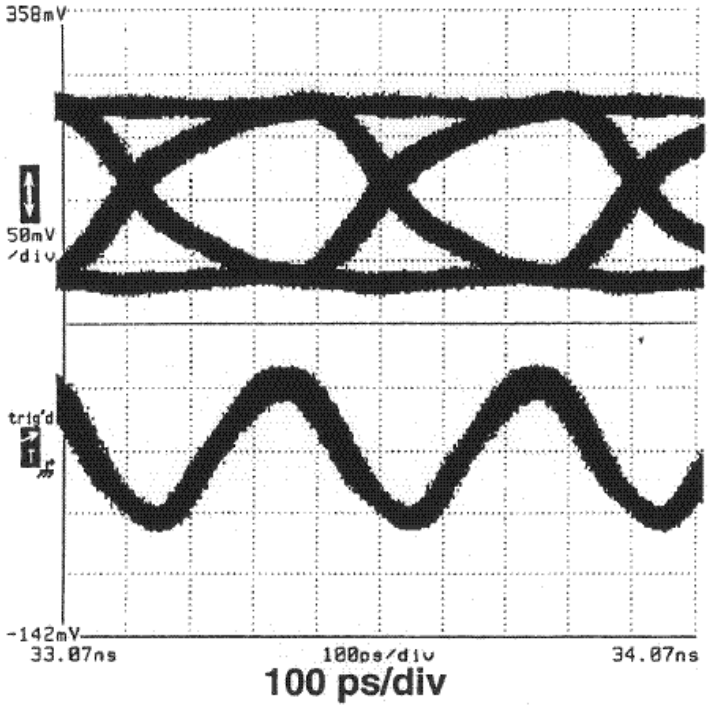
81 ps/div 20 ps/div

Recovered Clock Spectrum



500 kHz/div

Eye Diagram



Theoretical Jitter versus Measured Jitter

Phase Noise

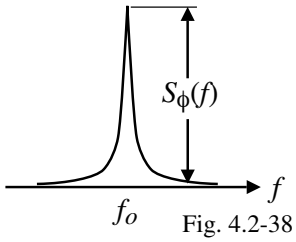


Fig. 4.2-38

- Measured free-running VCO phase noise = -85 dBc/Hz
- Closed-loop bandwidth = 3.1 MHz
- Theoretical closed-loop jitter = 5.08 ps

TimingJitter

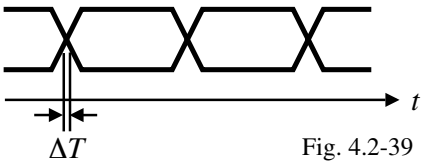


Fig. 4.2-39

Experimental closed-loop jitter = 5.1 ps

Summary of Experimental Results

Specification	Value
Bit Rate	2.5 Gb/s
Capture Range	540 MHz
Phase Noise at 1-MHz Offset	-92 dBc/Hz
Jitter for PRBS 2^{23}-1	5.1 ps
Power Dissipation: VCO VCO Buffer Phase detector and charge pump Frequency detector and comparator Total	 11mW 8mW 28.5mW 7.5mW 55mW
Supply Voltage	2.5V
Die Area	0.9 mm x 0.6 mm
Technology	0.25 μm CMOS

Summary of 2.5 Gb/s Example

- A method to resolve the conflict between a wide tuning range and low VCO sensitivity is described utilizing a dual-loop topology.
- An LC-based VCO with a segmented capacitor array is used to discretely tune the oscillation frequency.
- A charge pump that reduces drift in the event of no UP or DOWN pump signal is introduced.
- A method is proposed to estimate the closed-loop jitter based on the phase noise of the free-running VCO.

(To be continued)

